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MS-7818-1.1

Intel Shark Bay Plamform Z87

CPU:

Marswell LGA1150

System Chipset:

Lynx Point

Onboard Chip:

HD Audio:ALC1150

SIO:Fintek NTC6799D

LAN-E2205

Flash ROM: SPI 64 MB x2

Main Memory:

*DDRIII (800/1066/1333MHz) * 4 (Dual Channel)*

Expansion Slots:

PCI Express (X16) Slot x3

PCI Express (X1) Slot x4

Other:

SATA3.0 x8

REAR USB2.0 x2

FRONT USB2.0 x6

REAL USB3.0 x6

FRONT USB3.0 x2

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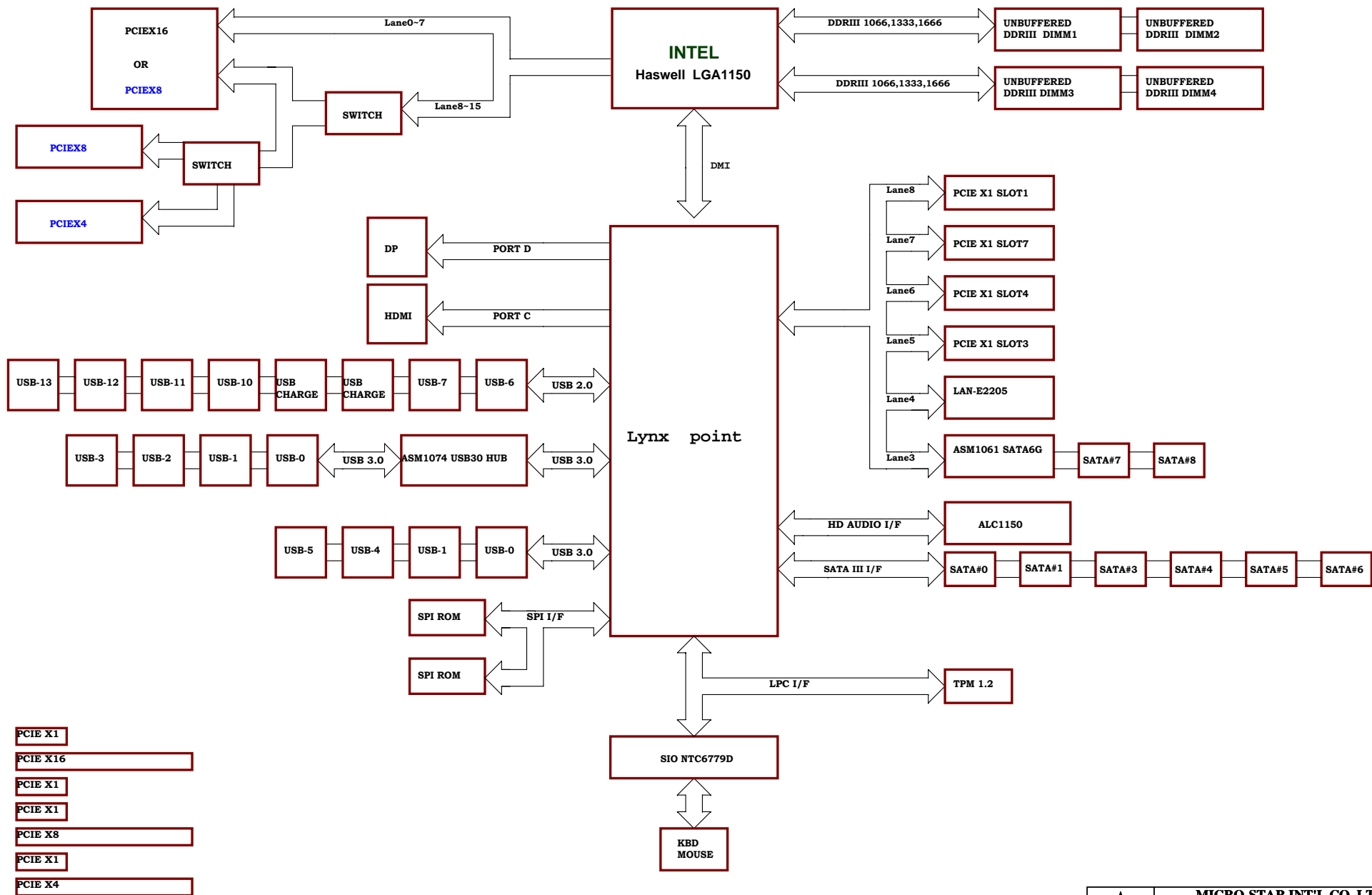
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Cover Sheet

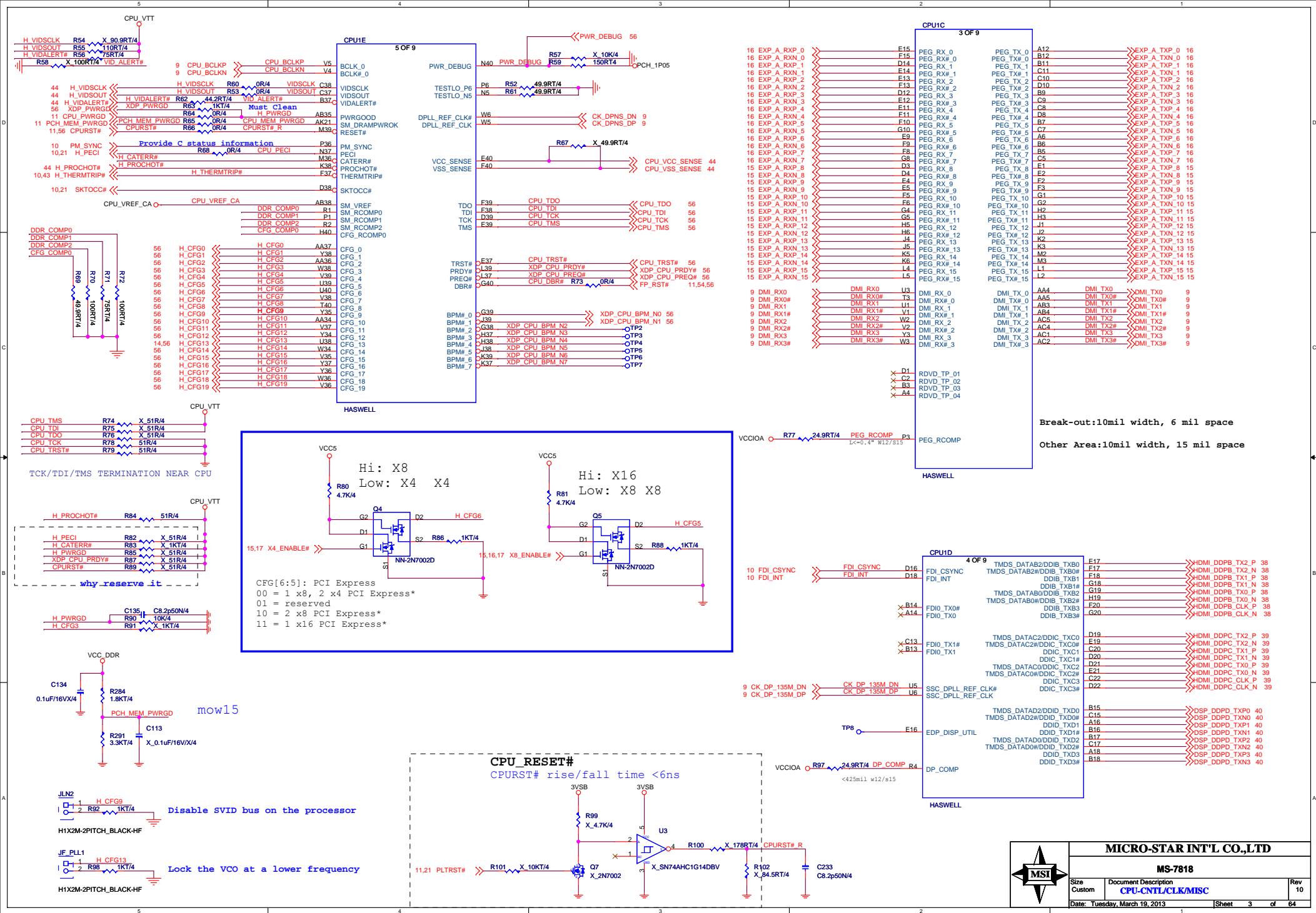
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- PCIE X1
- PCIE X16
- PCIE X1
- PCIE X1
- PCIE X8
- PCIE X1
- PCIE X4



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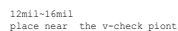
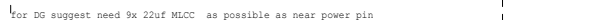
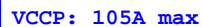
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CPU-CNTL/CLK/MISC

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Rev	10
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GND

GND



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Custom	CPU-GND	10
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CPU1G

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J6	VSS_361
K1	VSS_362
K18	VSS_363
K20	VSS_364
K22	VSS_365
K24	VSS_366
K26	VSS_367
K28	VSS_368
K30	VSS_369
K34	VSS_370
K36	VSS_371
K4	VSS_372
K40	VSS_373
K7	VSS_374
L7	VSS_375
L12	VSS_376
L9	VSS_377
L11	VSS_378
L3	VSS_379
L13	VSS_380
L14	VSS_381
L35	VSS_382
L38	VSS_383
L8	VSS_384
M1	VSS_385
K17	VSS_386
M12	VSS_387
M14	VSS_388
M18	VSS_389
M16	VSS_390
M20	VSS_391
M22	VSS_392
M24	VSS_393
M26	VSS_394
M28	VSS_395
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M32	VSS_397
M34	VSS_398
M37	VSS_399
M4	VSS_400
M40	VSS_401
M6	VSS_402
M5	VSS_403
M7	VSS_404
K15	VSS_405
K16	VSS_406
N1	VSS_407
N2	VSS_408
N3	VSS_409
N7	VSS_410
N34	VSS_411
N4	VSS_412
N6	VSS_413
K32	VSS_414
P2	VSS_415
P34	VSS_416
P38	VSS_417
P5	VSS_418
N8	VSS_419
R3	VSS_420
R36	VSS_421
R35	VSS_422
R40	VSS_423
R5	VSS_424
R6	VSS_425
R7	VSS_426
T1	VSS_427
T2	VSS_428
T3	VSS_429
T33	VSS_430
M35	VSS_431
T30	VSS_432
T4	VSS_433
T5	VSS_434
T6	VSS_435
T7	VSS_436
R8	VSS_437
U2	VSS_438
U33	VSS_439
U34	VSS_440
U37	VSS_441
U4	VSS_442
U7	VSS_443
AR5	VSS_444
P35	VSS_445
V33	VSS_446
V40	VSS_447
V6	VSS_448
V8	VSS_449
W1	VSS_450
W33	VSS_451
W35	VSS_452
W37	VSS_453
W4	VSS_454
W7	VSS_455
Y33	VSS_456
Y4	VSS_457
Y5	VSS_458
Y6	VSS_459

HASWELL

VSS_0270

C36

C23

C21

C19

C18

C16

C14

C12

C6

C4

B8

B4

B36

B34

B30

B28

B26

B24

AY7

AY5

AY30

AY27

AY26

AY23

AY17

AW7

AW36

AW34

AW32

AW30

AW3

AW26

AV7

AV38

AV34

AV30

AV3

AV28

AV21

AU7

AU5

AU38

AU34

AU30

AU3

AU25

AU2

AT9

AT8

AT7

AT6

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AR5

AR40

AR39

AR38

AR37

AR36

AR35

AR34

AR33

AR32

AR31

AR30

AR27

AR24

VSS_0181

VSS_0182

VSS_0183

VSS_0184

VSS_0185

VSS_0186

VSS_0187

VSS_0188

VSS_0189

VSS_0190

VSS_0191

VSS_0192

VSS_0193

VSS_0194

VSS_0195

VSS_0196

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VSS_0198

VSS_0199

VSS_0200

VSS_0201

VSS_0202

VSS_0203

VSS_0204

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VSS_0206

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VSS_0211

VSS_0212

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VSS_0237

VSS_0238

VSS_0239

VSS_0240

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VSS_0242

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VSS_0244

VSS_0245

VSS_0246

VSS_0247

VSS_0248

VSS_0249

VSS_0250

VSS_0251

VSS_0252

VSS_0253

VSS_0254

VSS_0255

VSS_0256

VSS_0257

VSS_0258

VSS_0259

VSS_0260

VSS_0261

VSS_0262

VSS_0263

VSS_0264

VSS_0265

VSS_0266

VSS_0267

VSS_0268

VSS_0269

VSS_0270

VSS_0271

VSS_0272

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VSS_0300

VSS_0301

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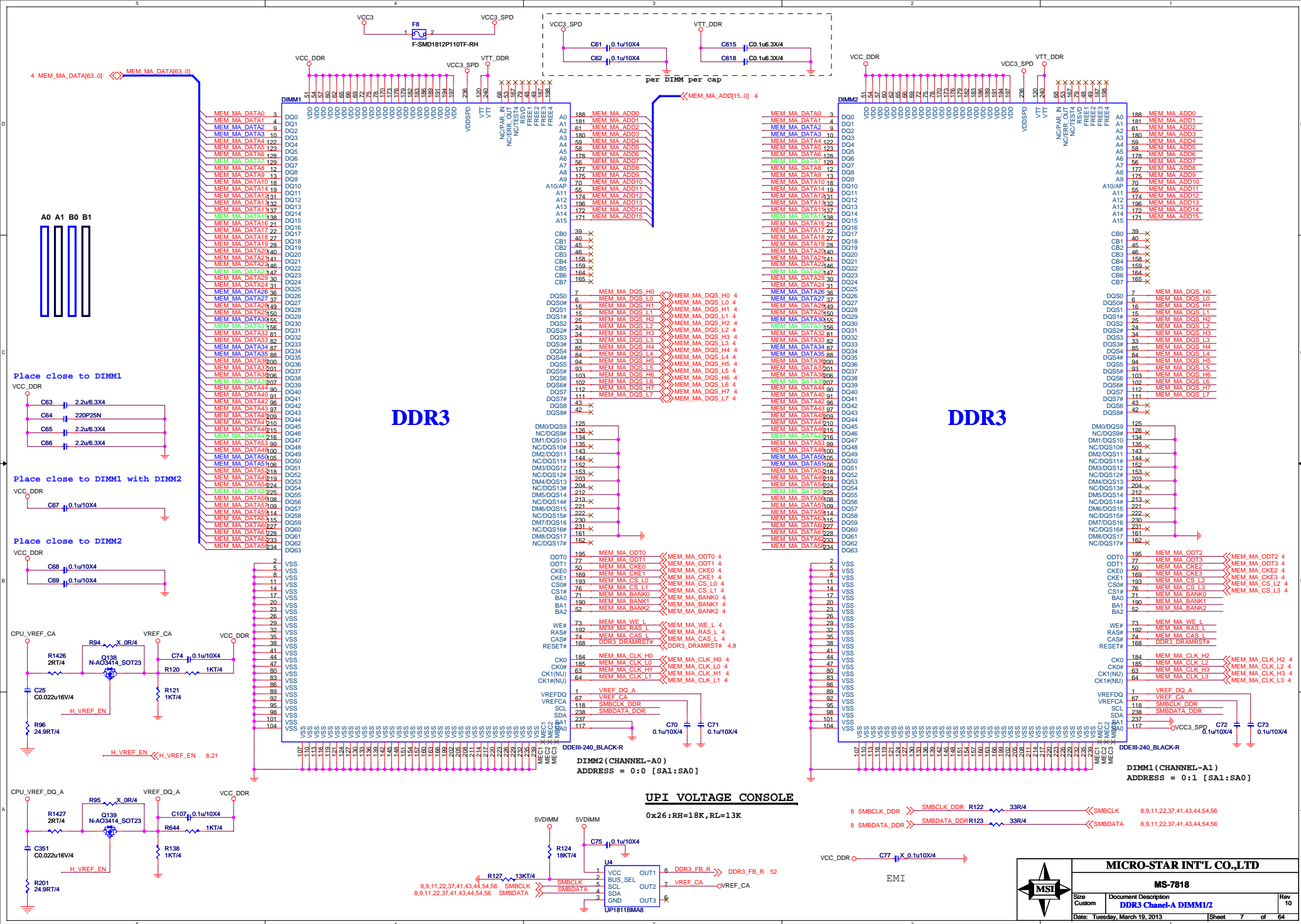
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VSS_0343

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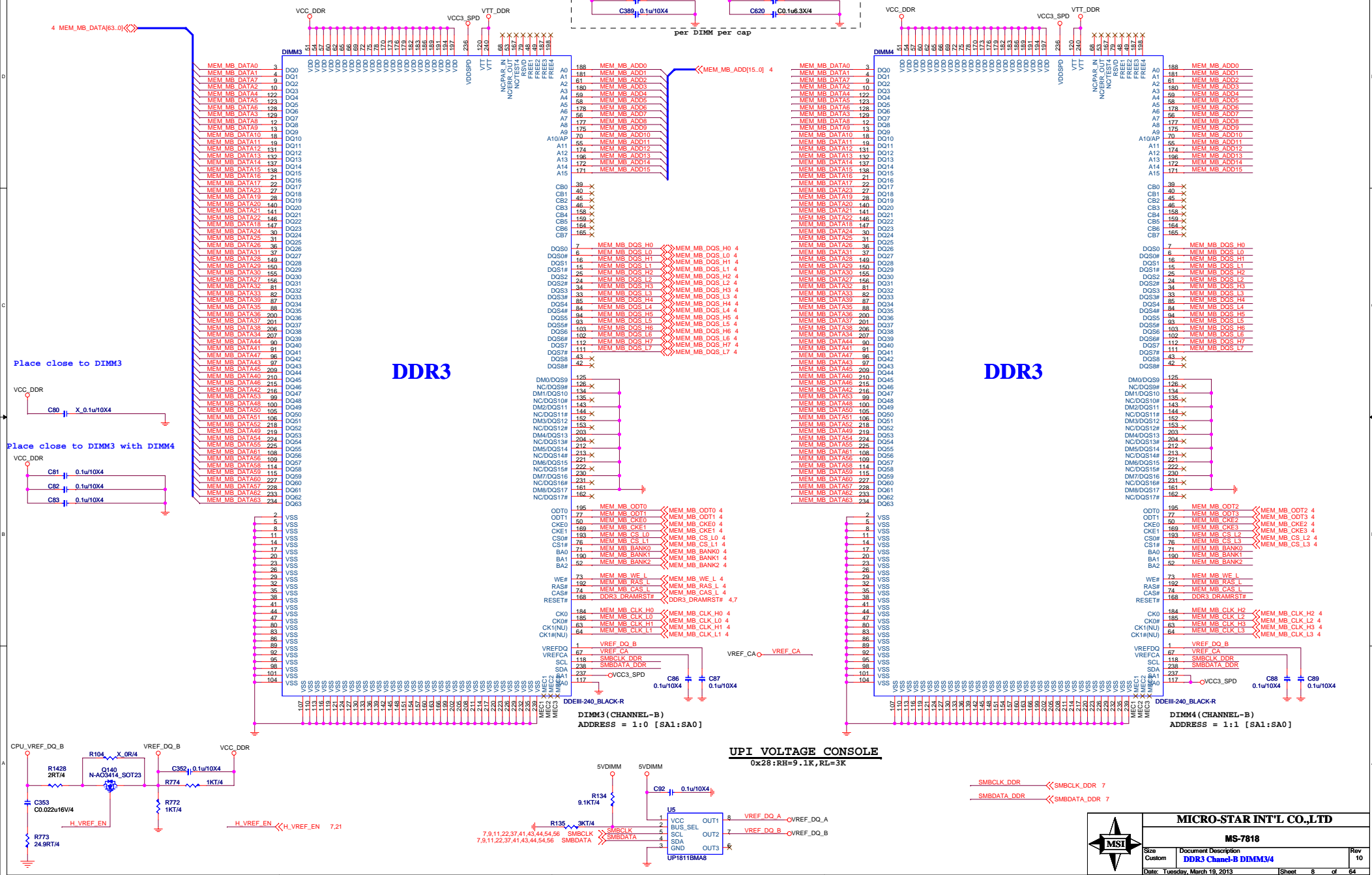


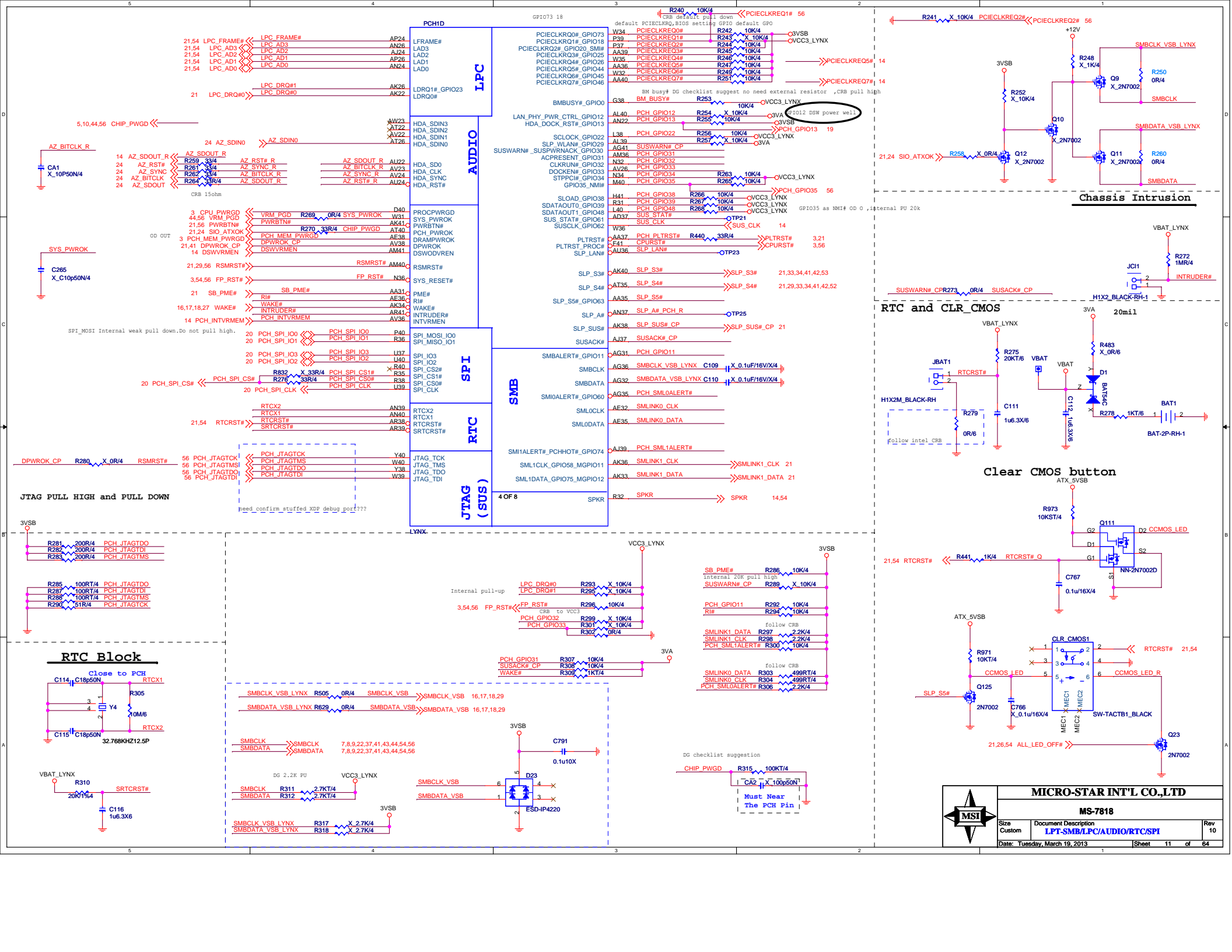
MS-7818

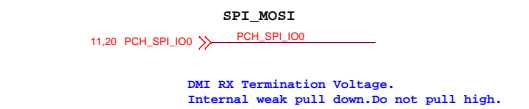
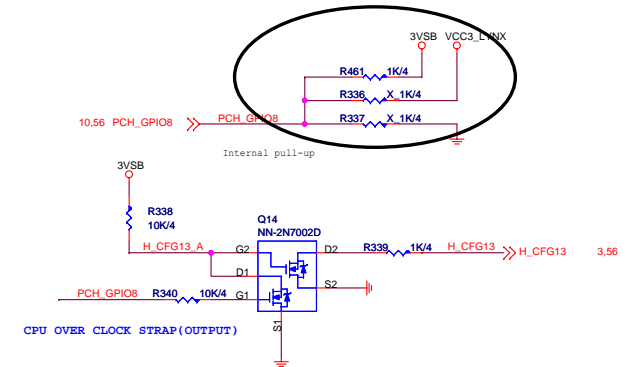
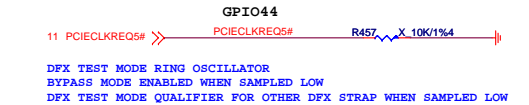
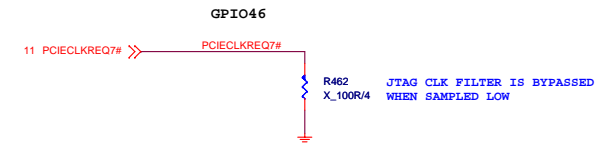
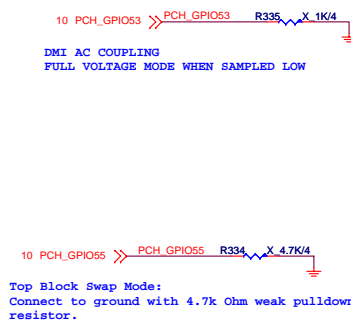
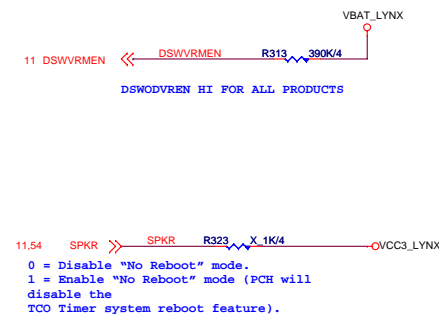
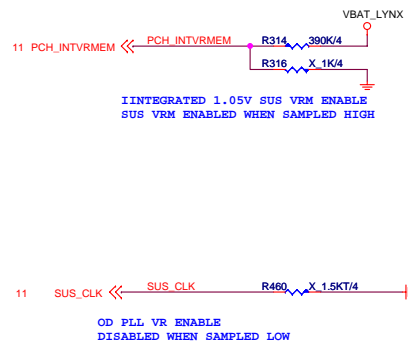
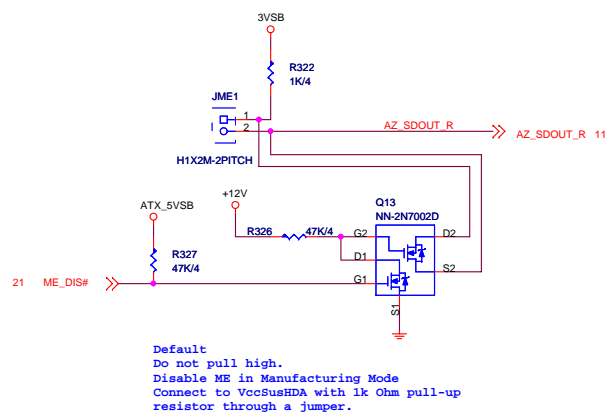
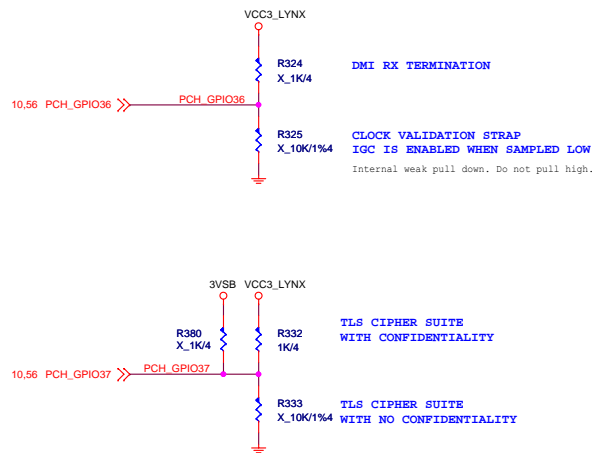
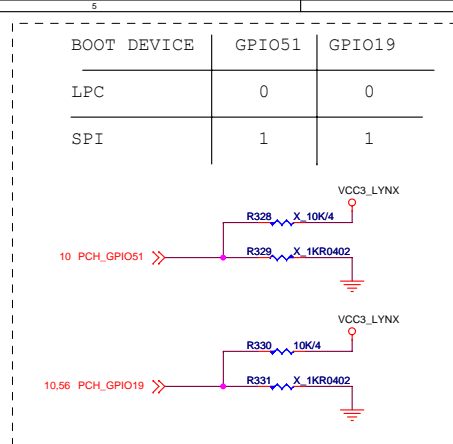
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DDR3 DIMM_B0

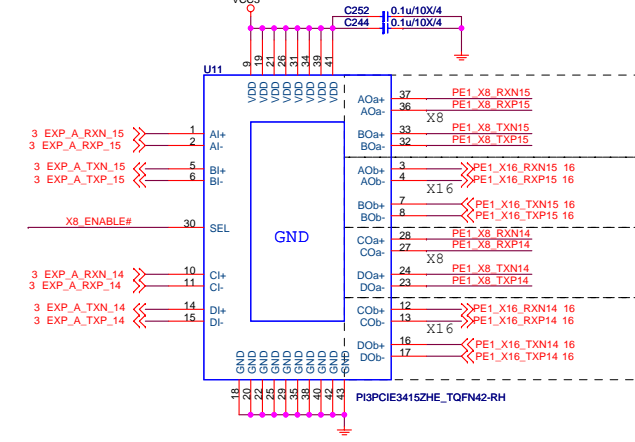
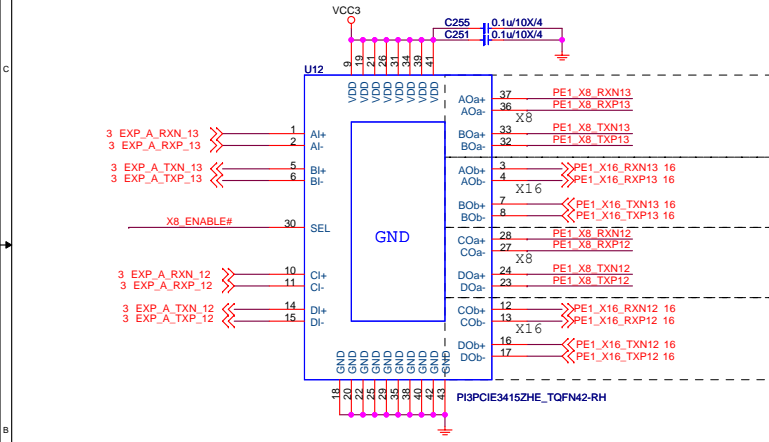
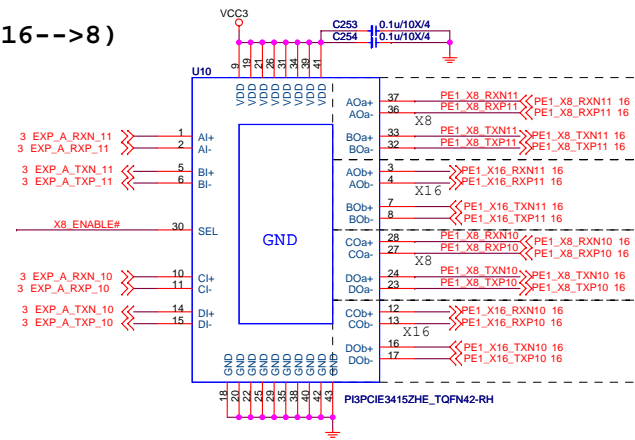
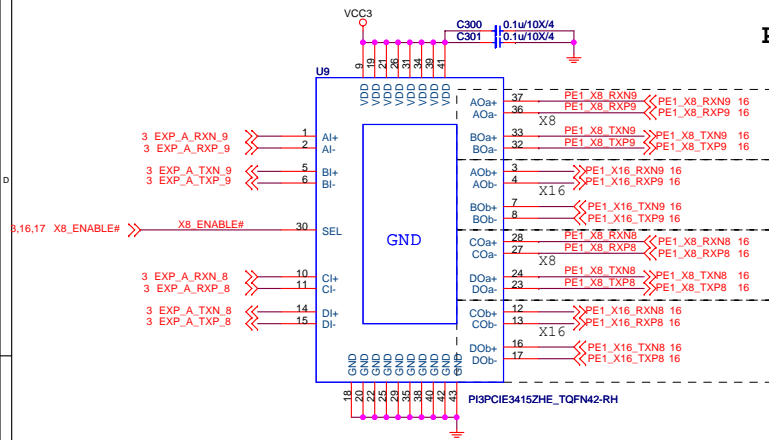
DDR3 DIMM_B1





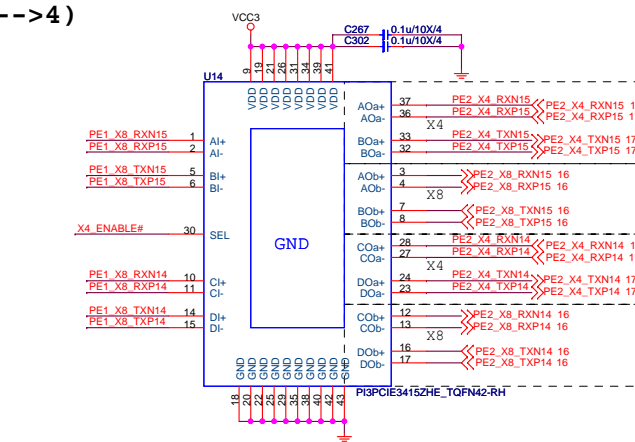
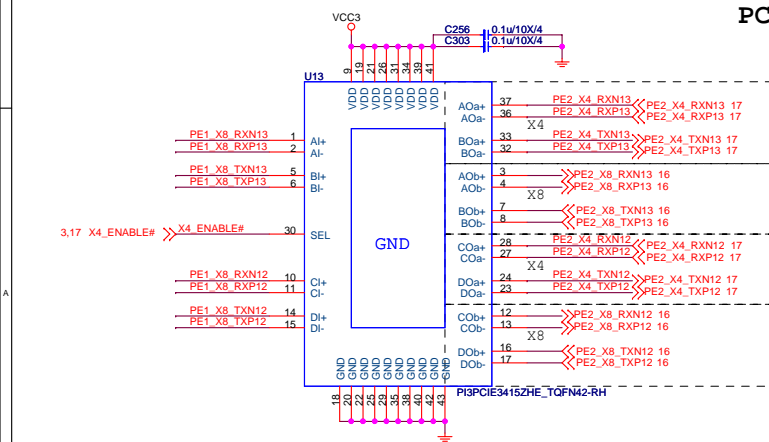


PCIE Switch (16-->8)



X8_ENABLE#	PCI-E_slot 1/2
Low	X8 / X8
Hi	X16

PCIE Switch (8-->4)

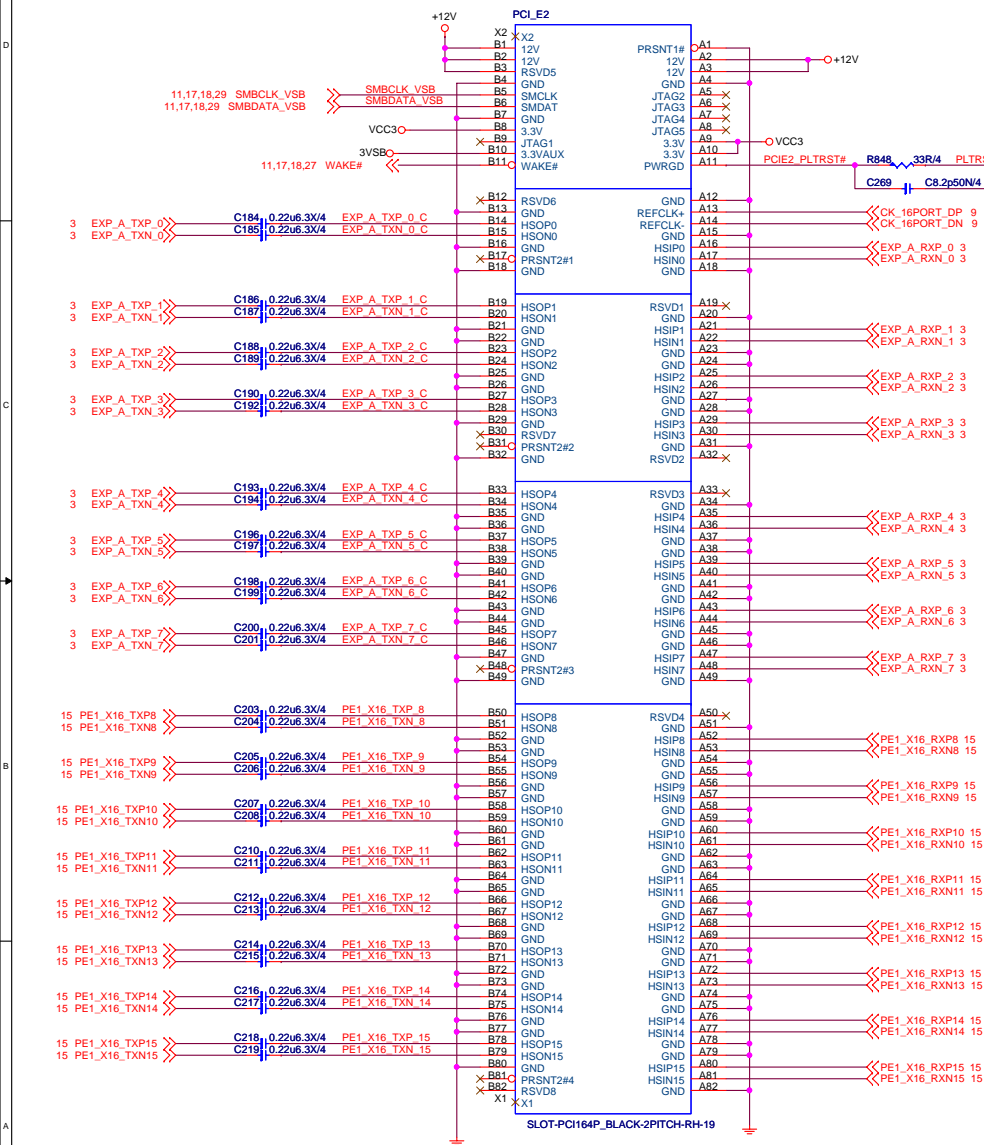


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Low	X4 / X4
Hi	X8

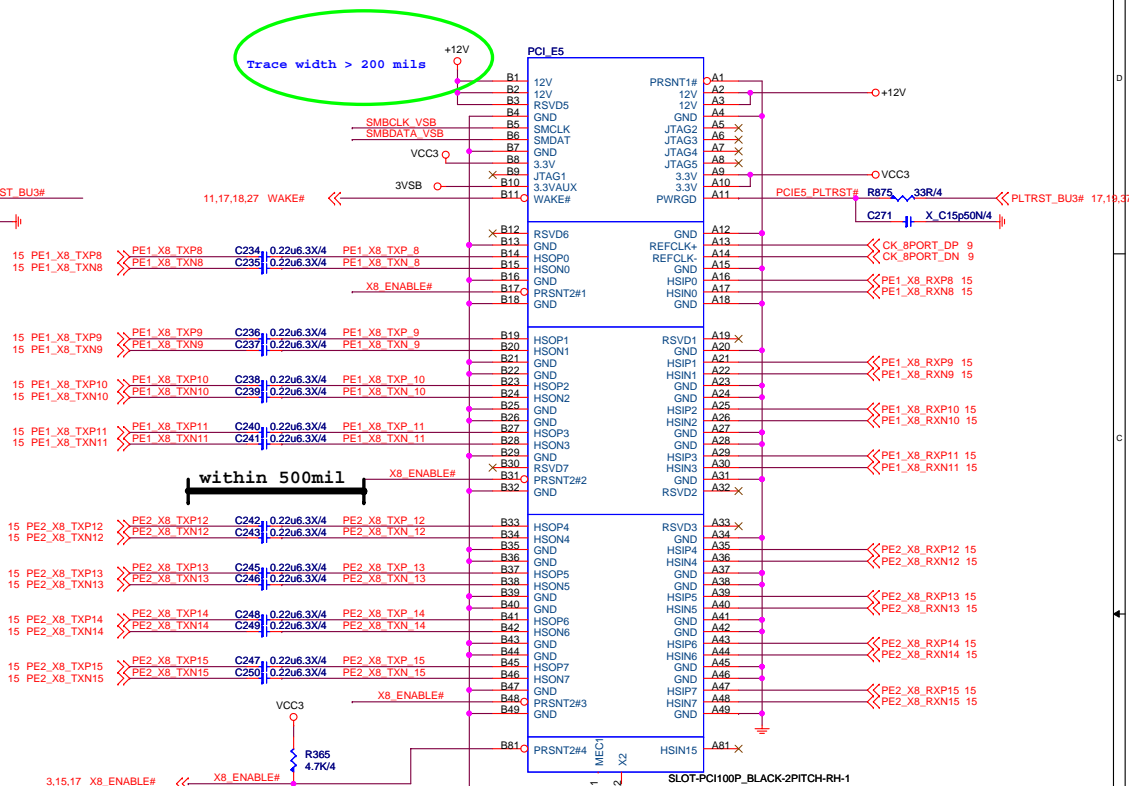


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Size Custom	Document Description PCIE SWITCH (16-->8)&(8-->4)	Rev 10
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PCI_Express X16 Slot
(Share with PCI_E x8 Slots)



PCI_Express X8 Slot
(Share with PCI_E x16 Slots)



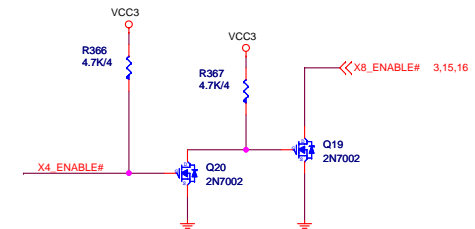
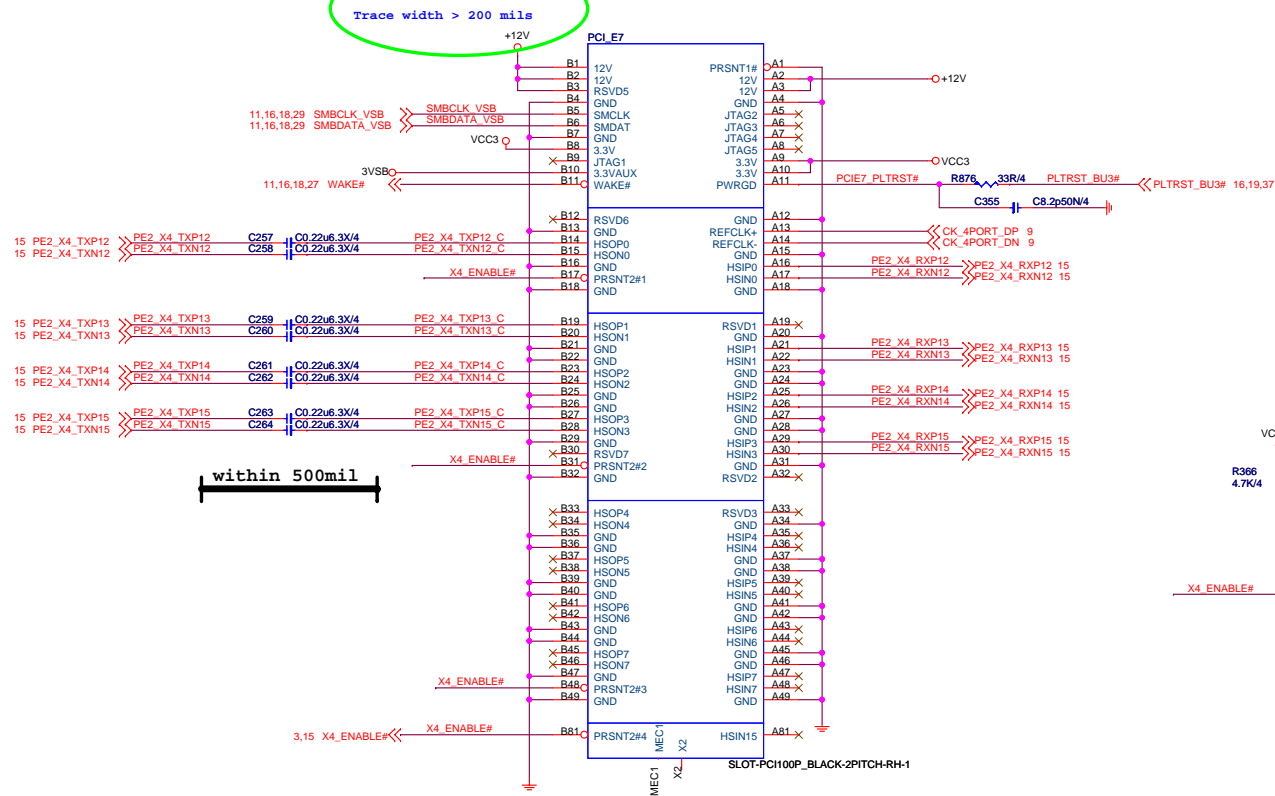
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Size	Document Description
Custom	PCIE X16 And X8 SLOTS

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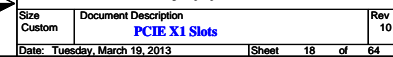
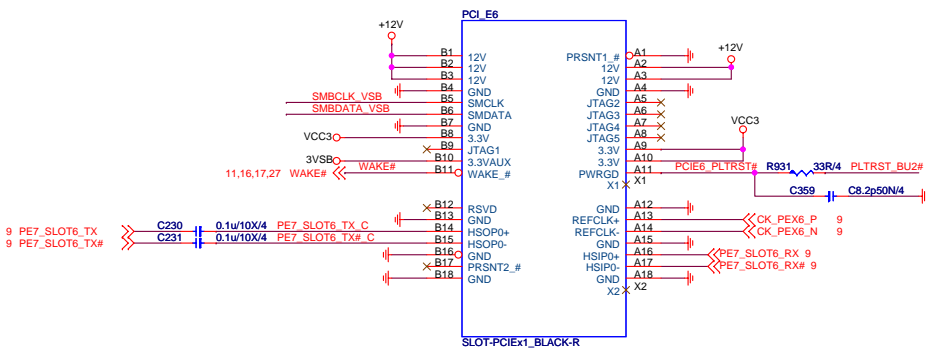
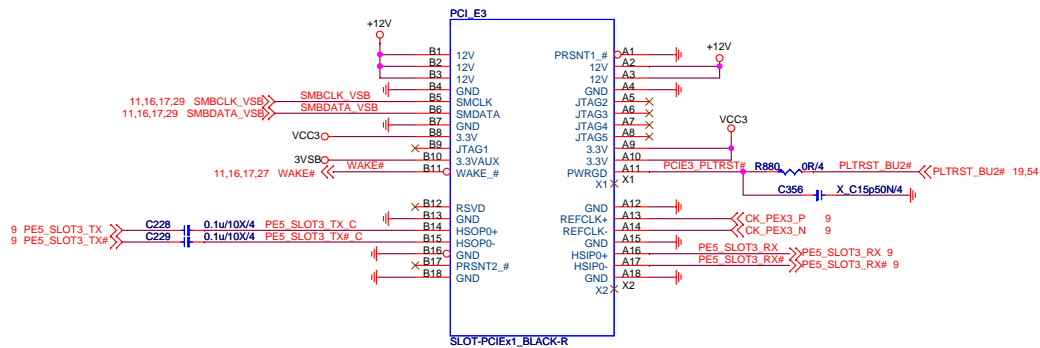
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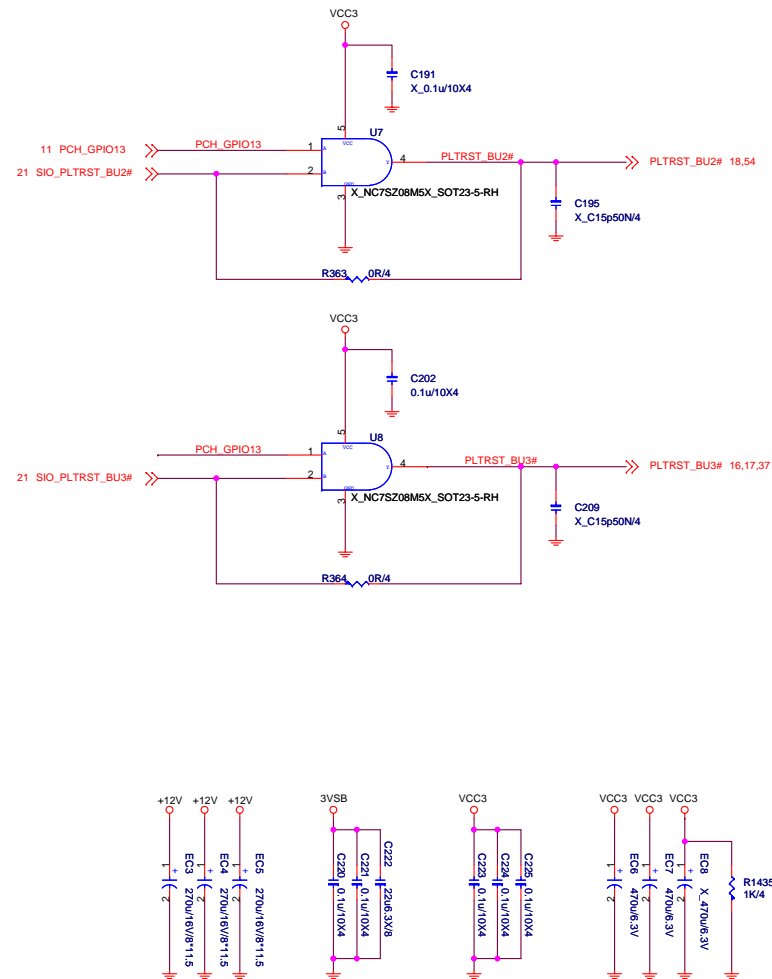


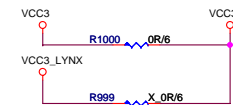
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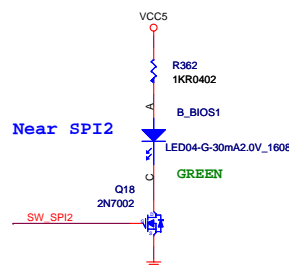
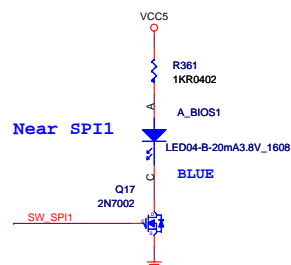
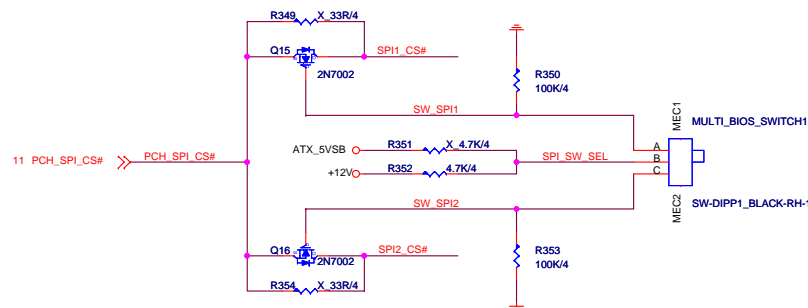
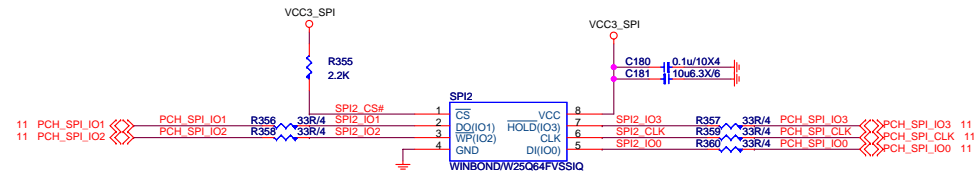
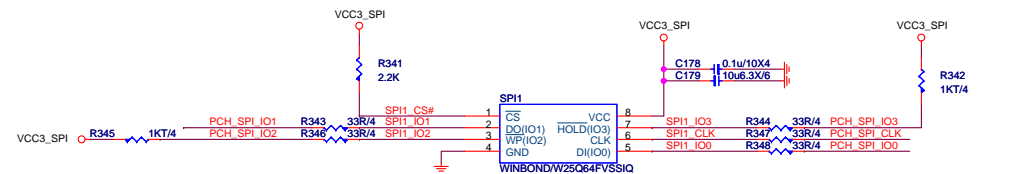




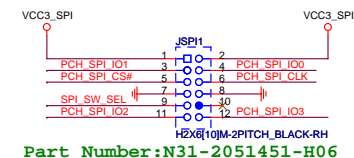


SPI FLASH ROM

Place close to SB.



Close to SPI ROM



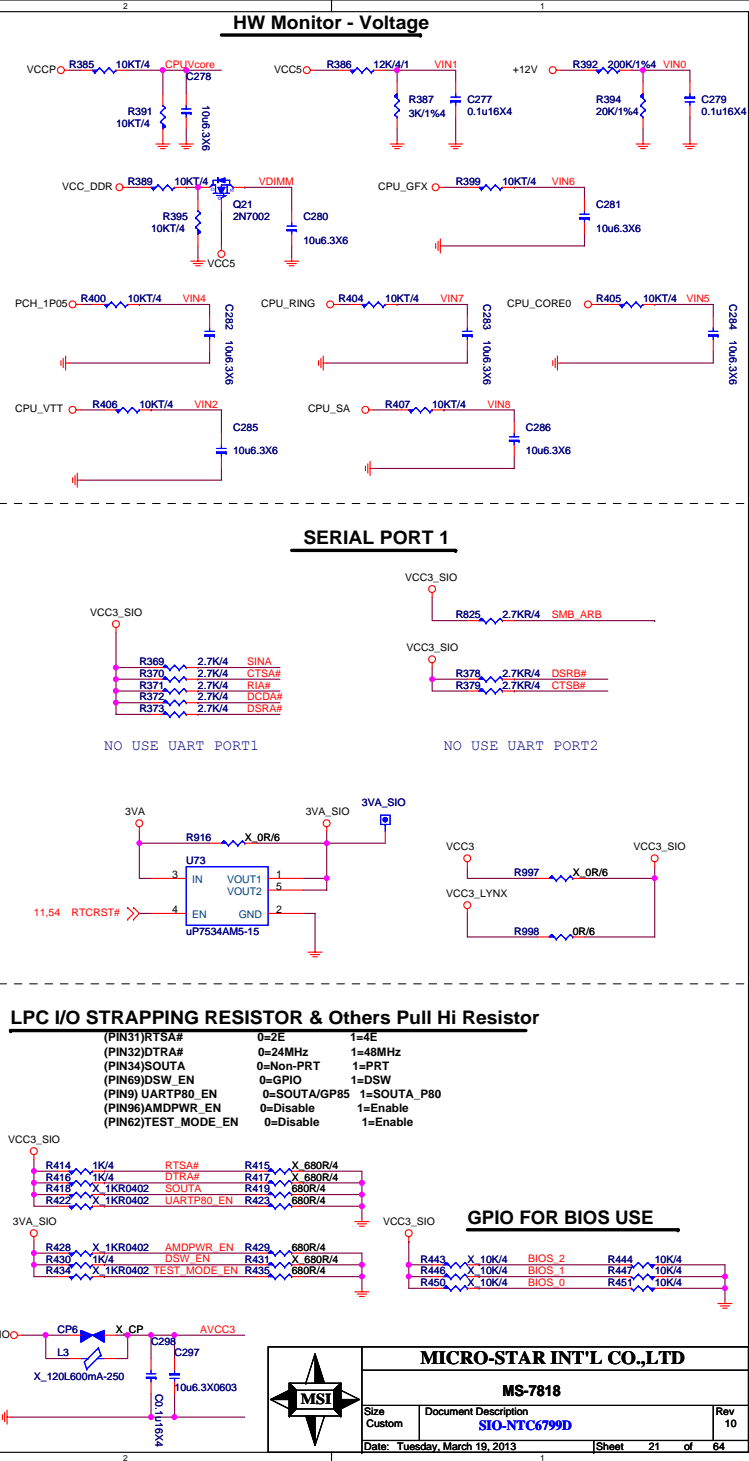
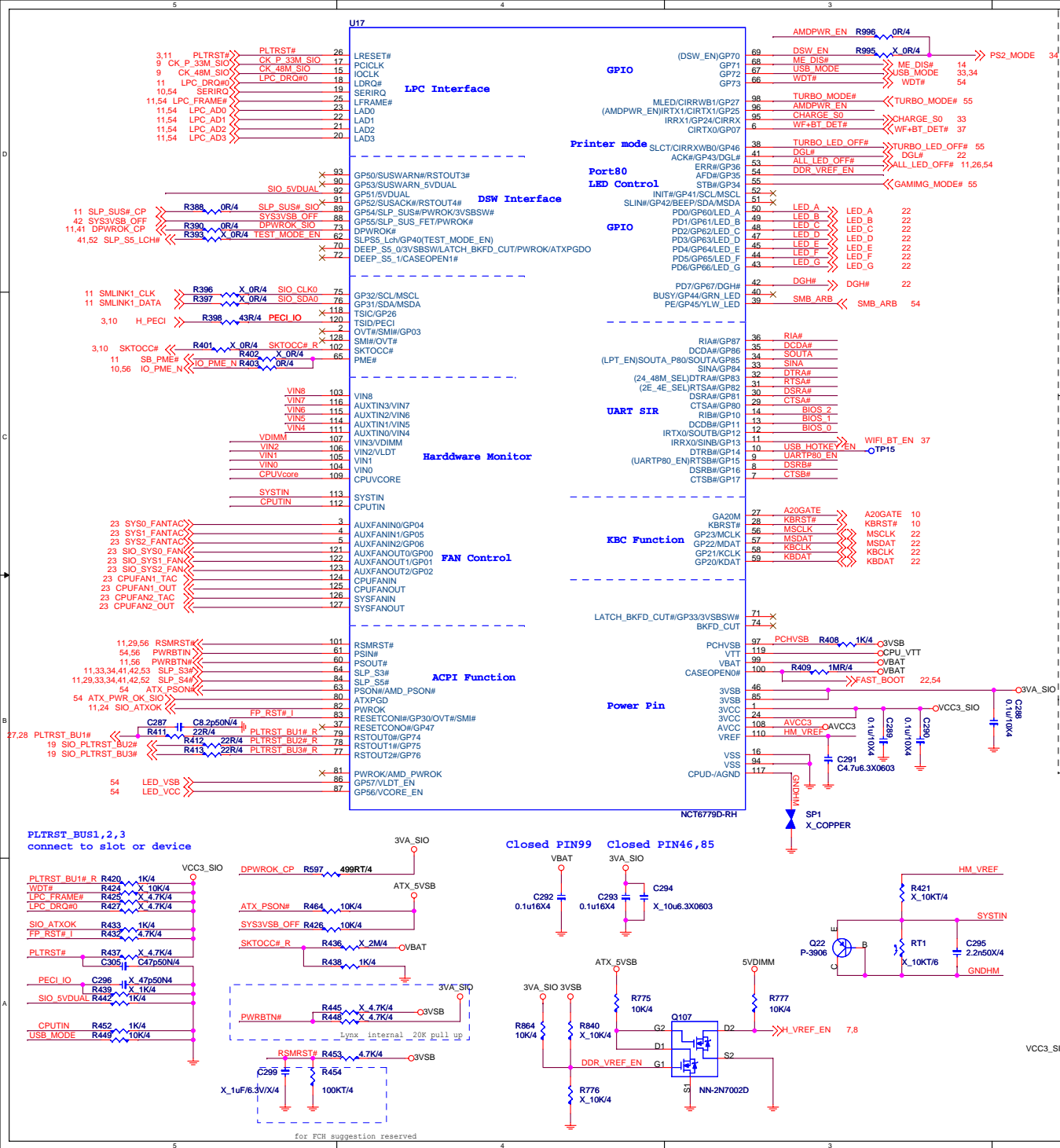
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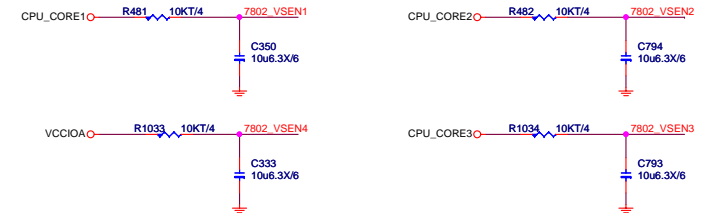
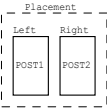


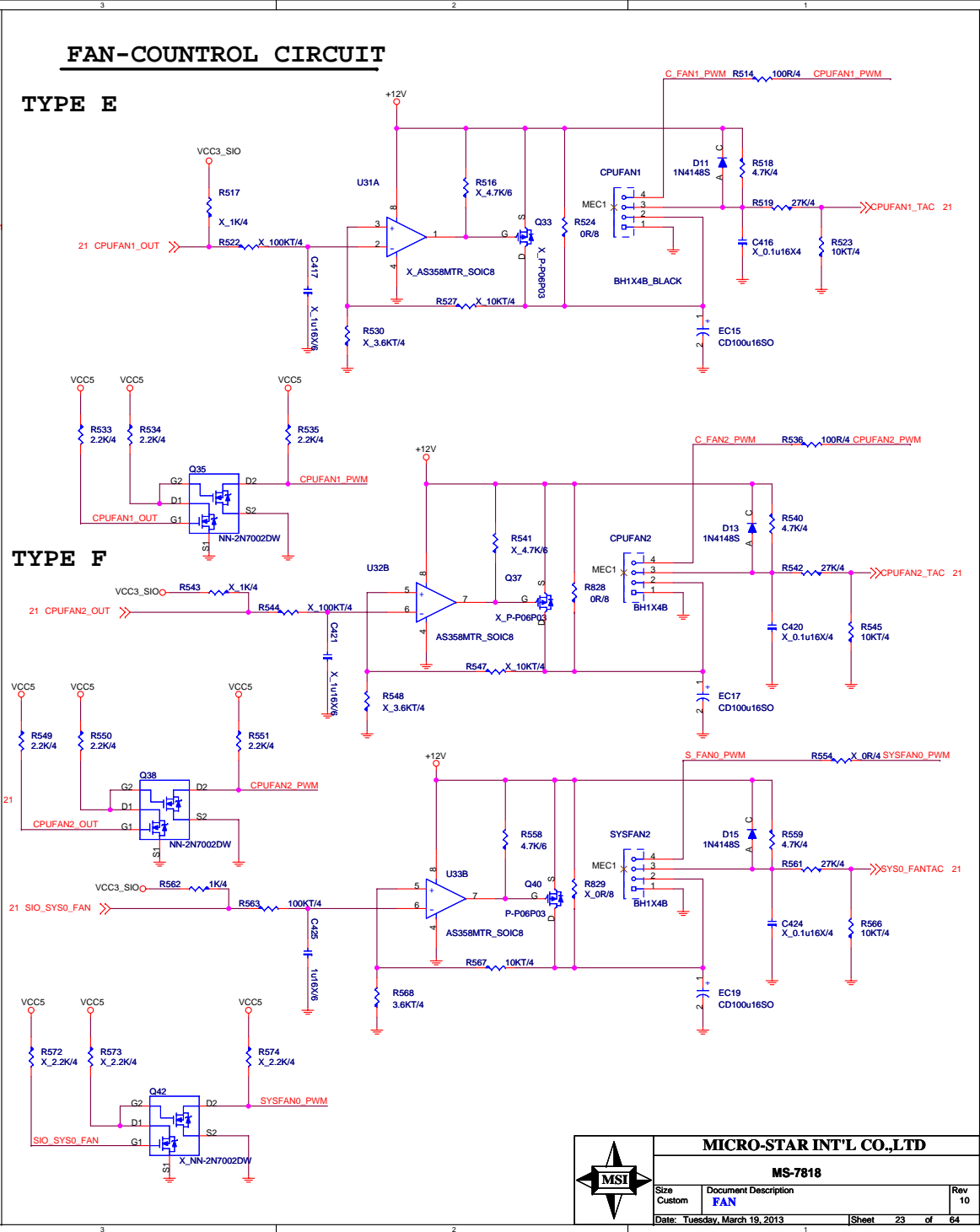
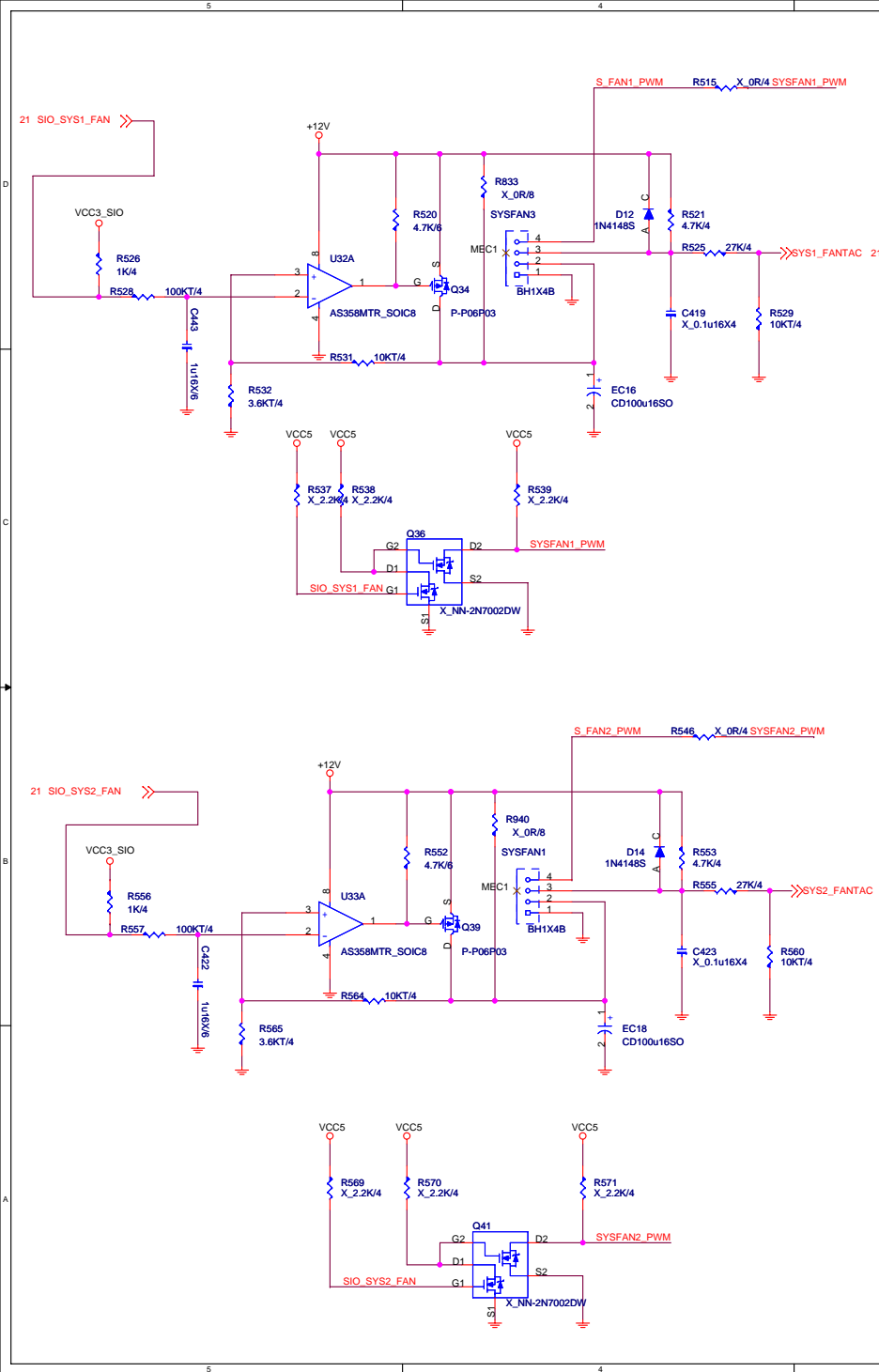
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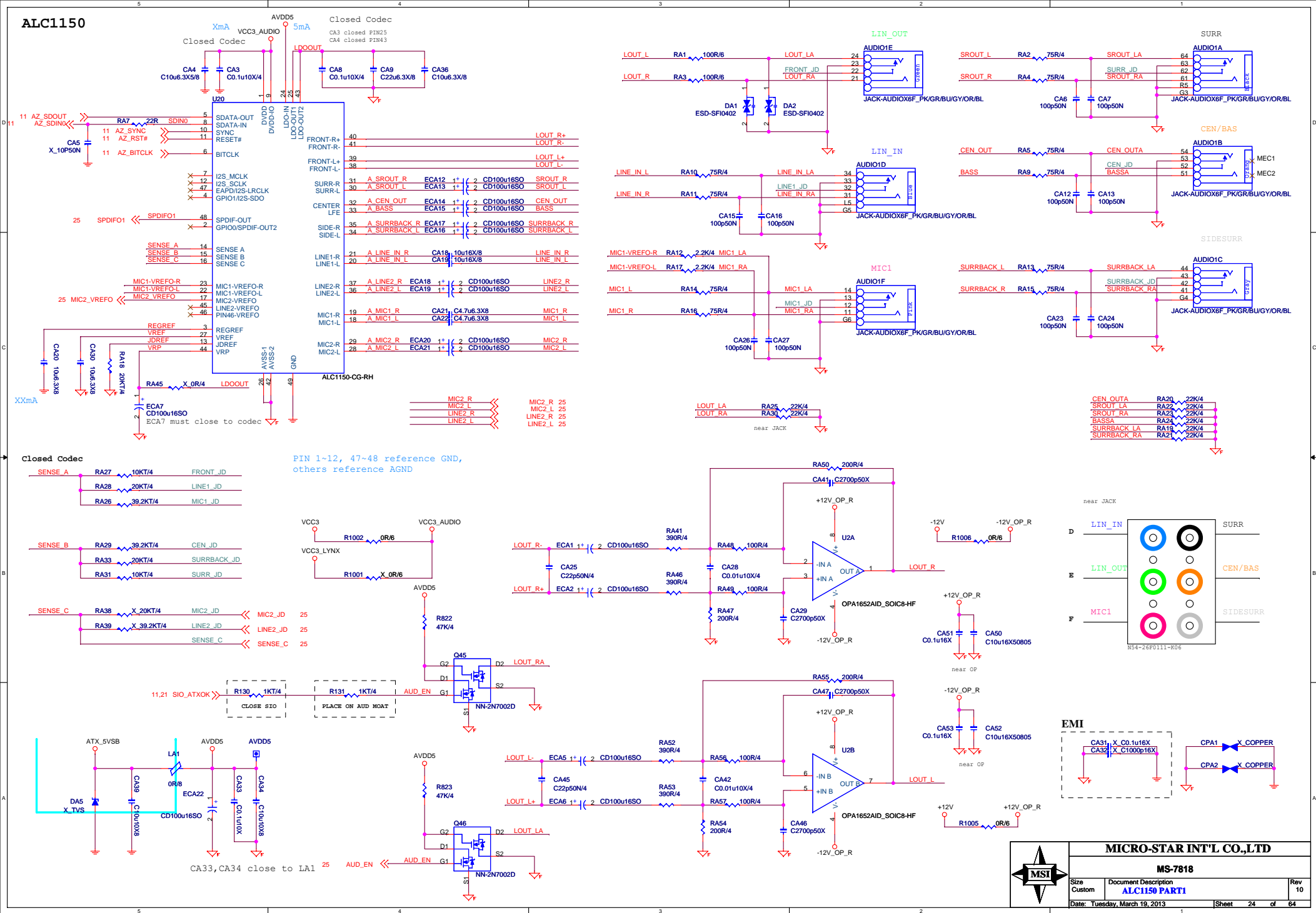


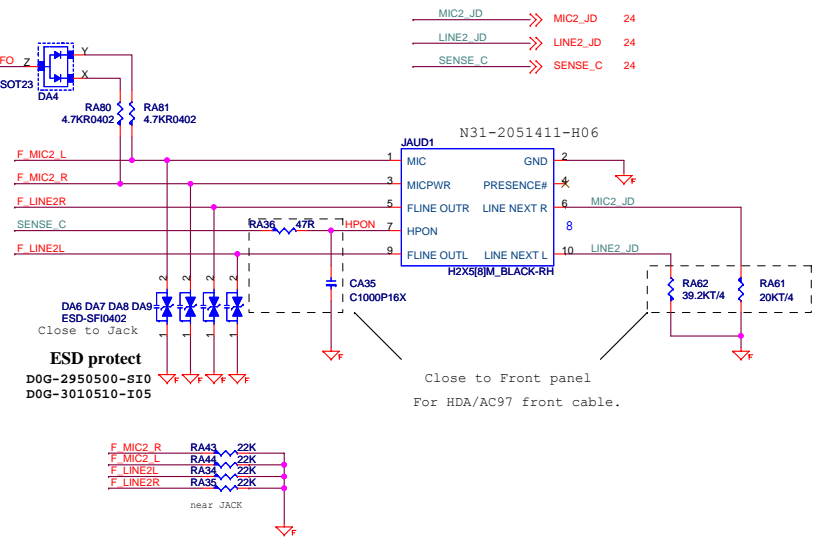
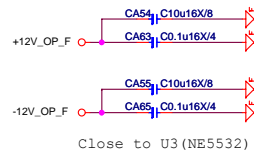
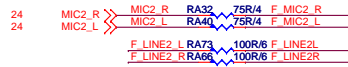
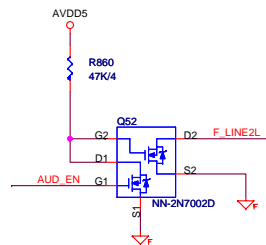
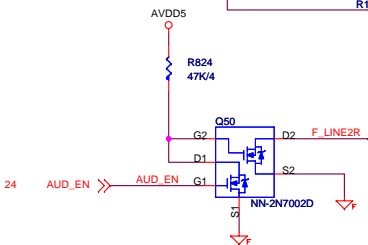
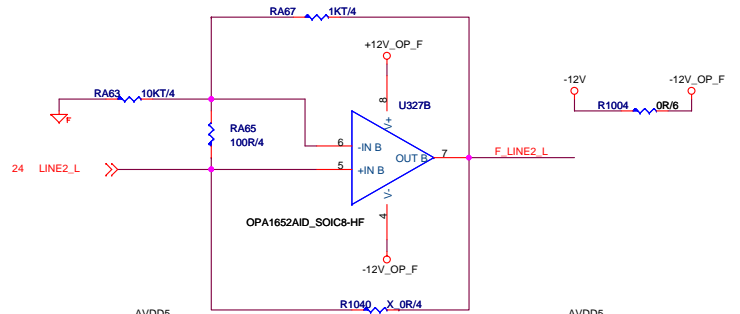
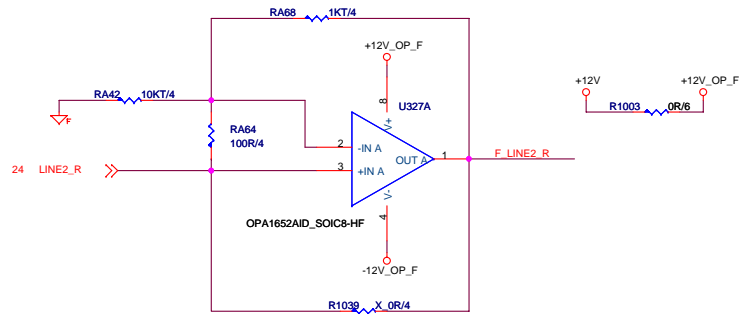
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MS-7818

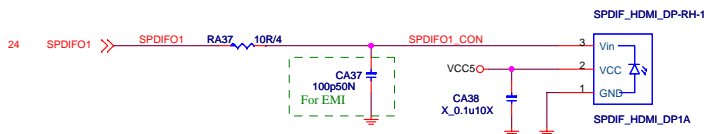
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ALC1150



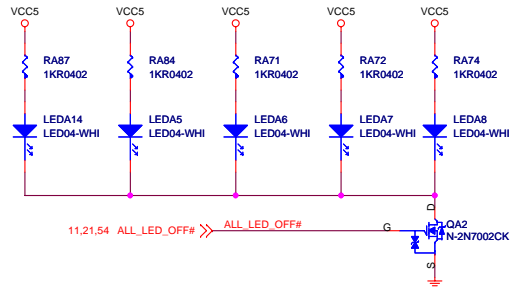
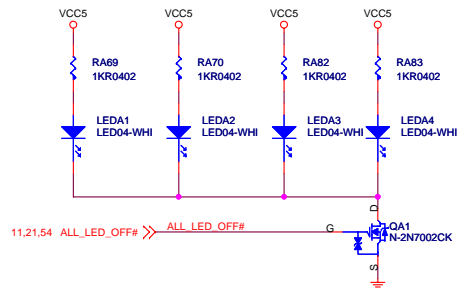


SPDIF OUT

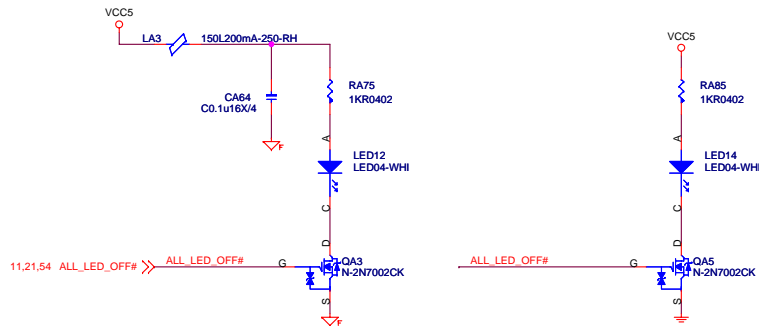


MICRO-STAR INT'L CO.,LTD		
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Size Custom	Document Description ALC1150 PART2	Rev 10
Date: Tuesday, March 19, 2013	Sheet 25 of 64	

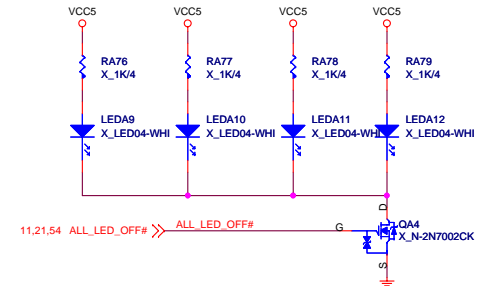
For AUDIO MOAT



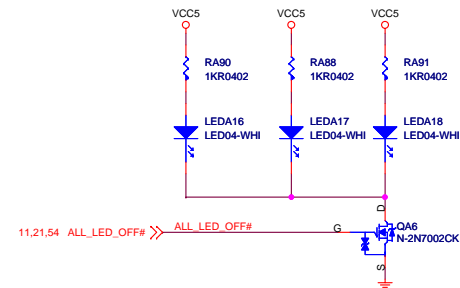
For AUDIO(TOP SIDE)



For MSI LOGO



For LYNX

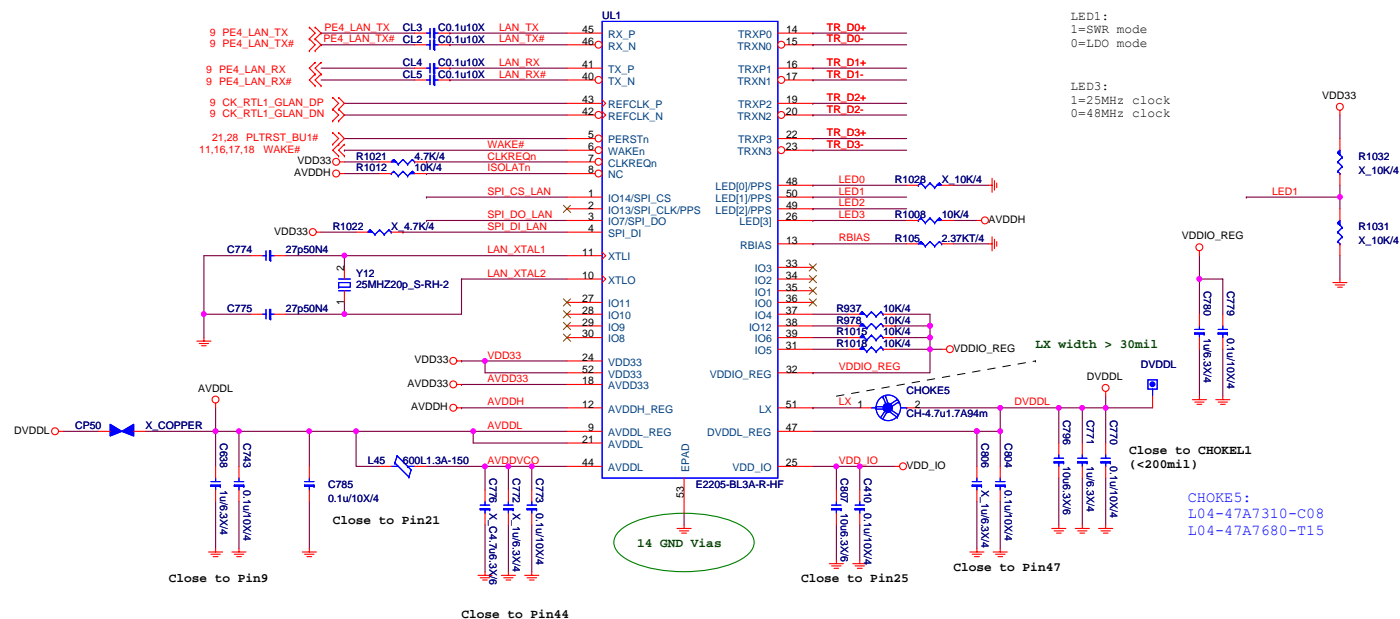


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Size Custom	Document Description LED LIGHT	Rev 10
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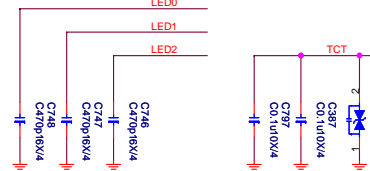
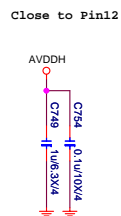
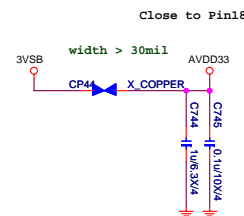
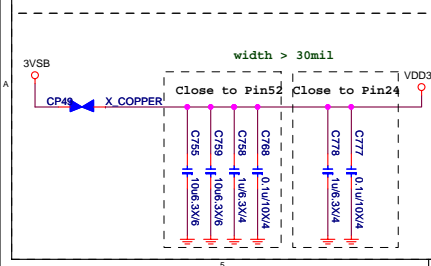
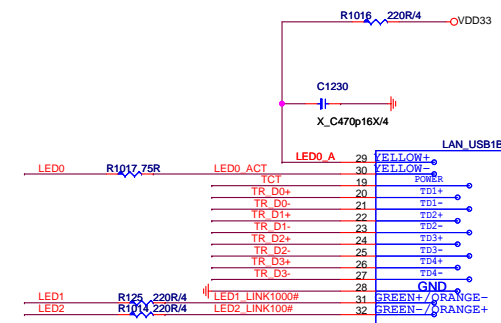
E2205-B Giga LAN



- ```

10:
1. Support xD, not support SPI
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFUS
01:
1. Support SPI, not support xD
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFUS
11:
1. Not support xD, not support SPI
2. Only support PPS, PPS always at CRI013.

```



RJ45\_USBX2\_LEDX2\_TX-RH-42

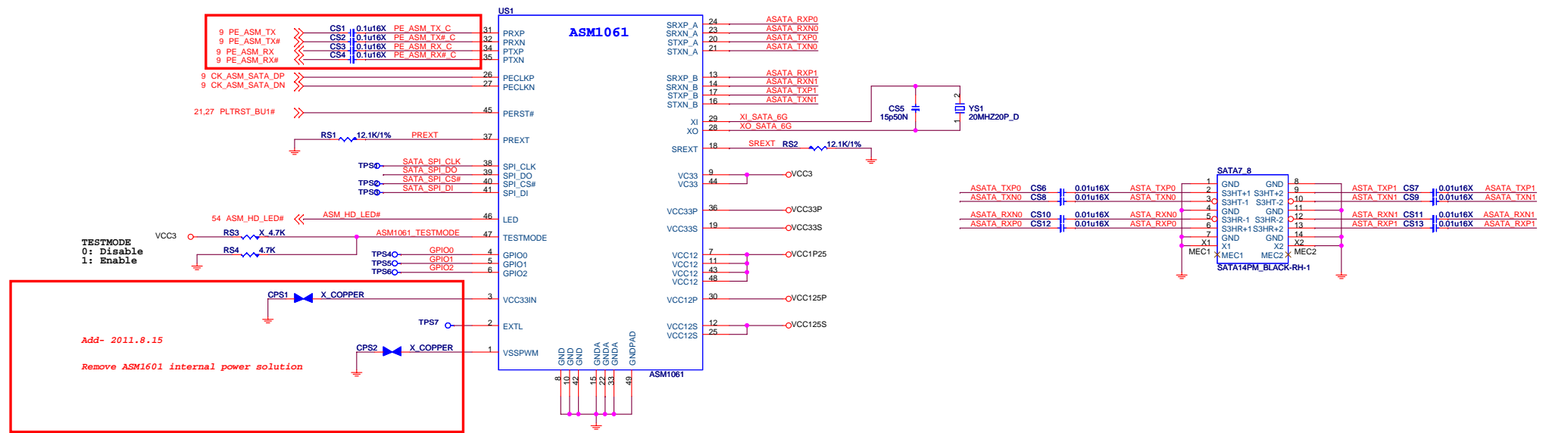


**MICRO-STAR INT'L CO.,LTD**

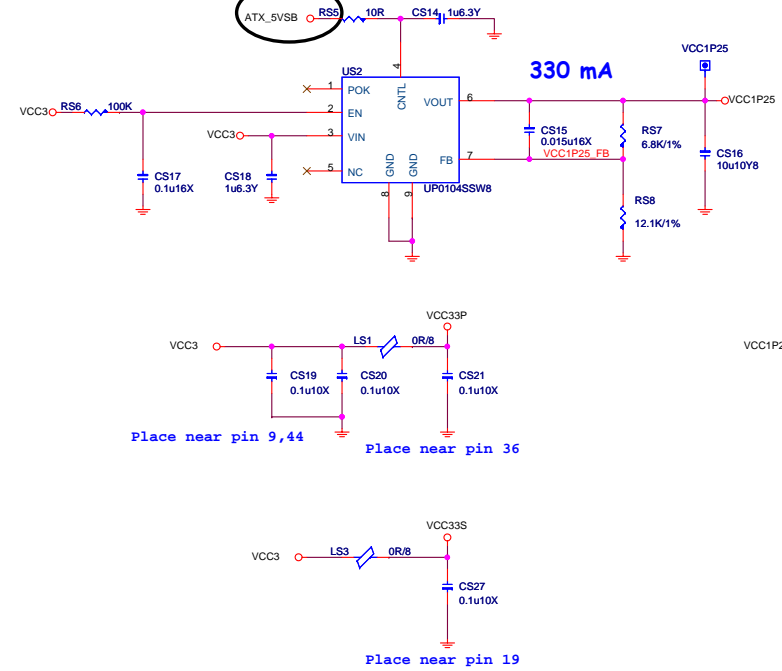
MS-7818

|                               |                                          |                |
|-------------------------------|------------------------------------------|----------------|
| Size<br>Custom                | Document Description<br><b>LAN-E2205</b> | Rev<br>10      |
| Date: Tuesday, March 19, 2013 |                                          | Sheet 27 of 64 |

ASM1061 SATA6G

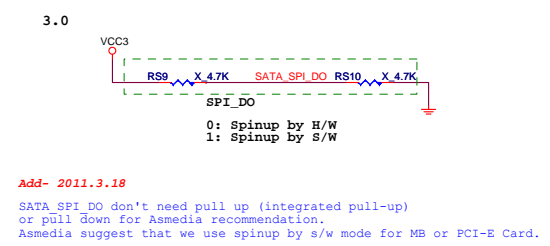


1.2V delay from 3.3V 90% > 0ms

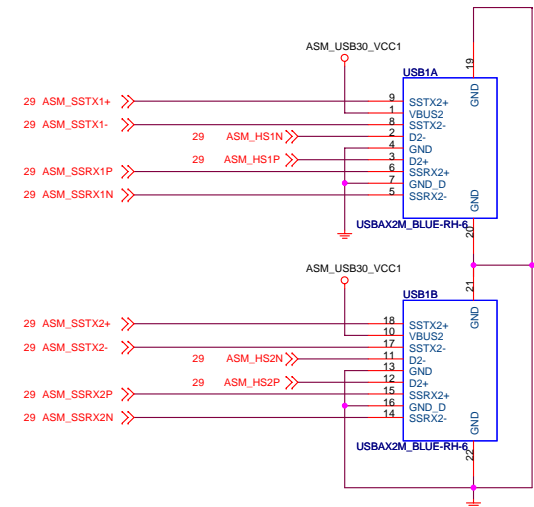
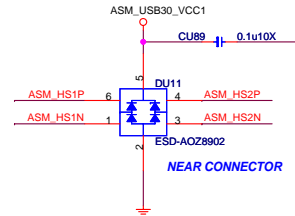
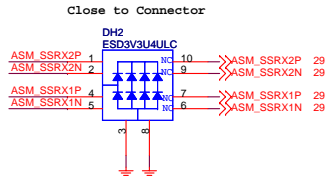
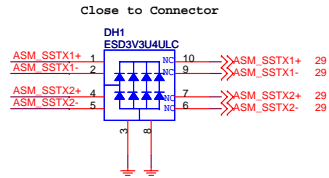


ASM1061 POWER Consumption

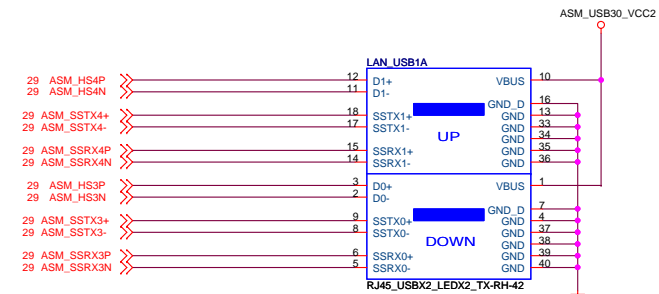
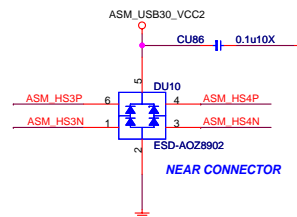
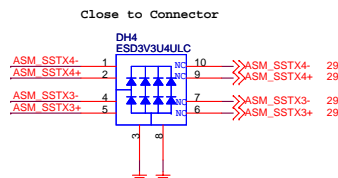
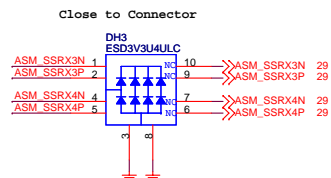
|           | 3.3V  | 1.2V  | Power (mW) |
|-----------|-------|-------|------------|
| Idle (mA) | 98.45 | 212.3 | 579.645    |
| Busy (mA) | 91.1  | 330.7 | 697.47     |







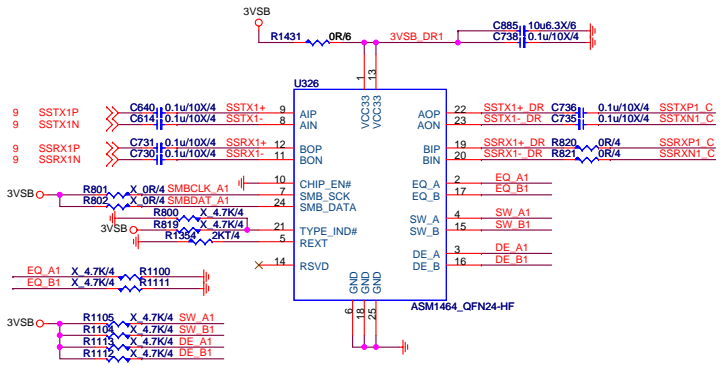
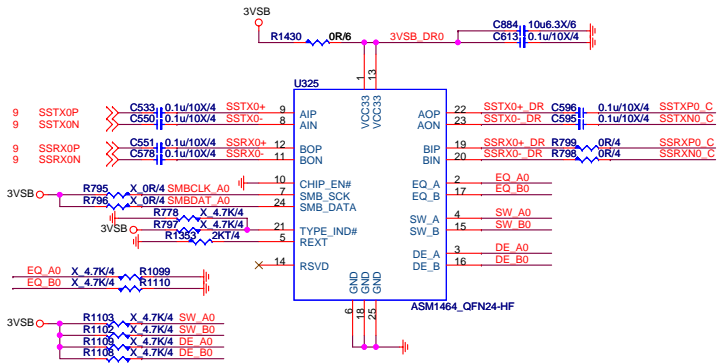
Important--  
If USB3.0 signal connect to front pin header,  
please must less than 2 inch, 1.5 inch is better.  
USB3.0 test will fail in factory if you aren't follow this rule.



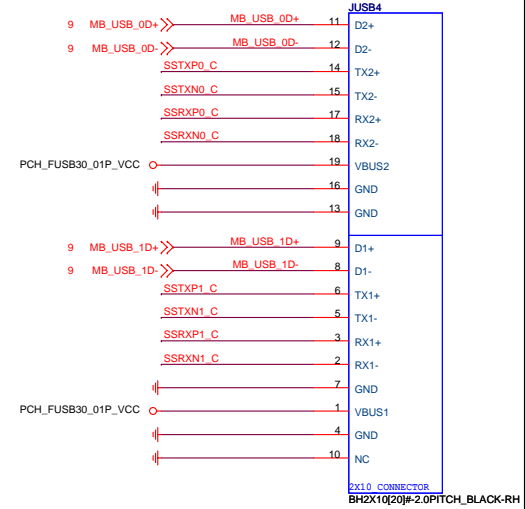
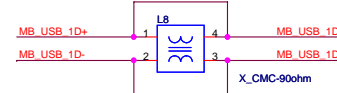
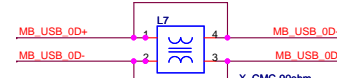
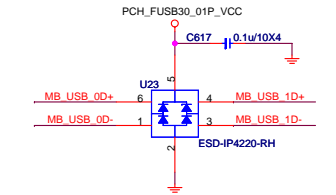
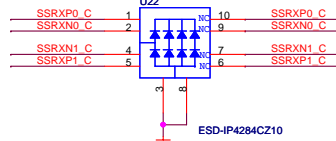
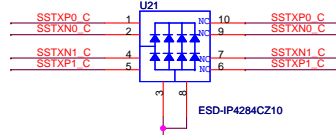
MICRO-STAR INT'L CO.,LTD

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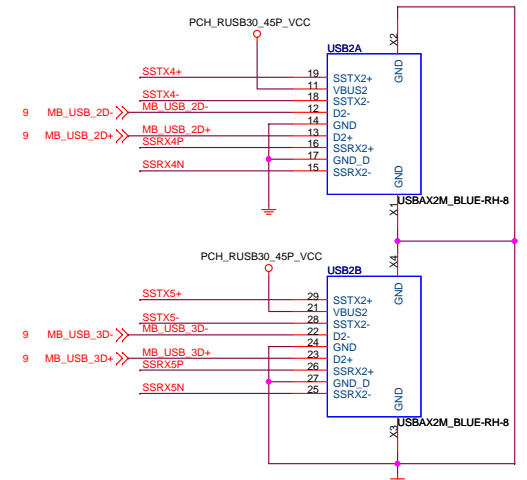
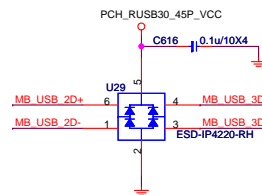
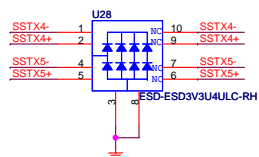
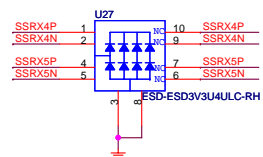
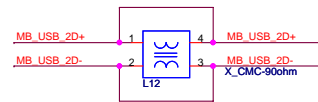
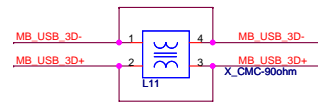
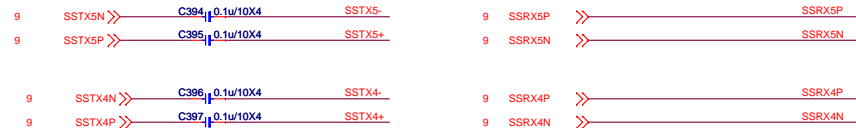
| Size                          | Document Description | Rev |
|-------------------------------|----------------------|-----|
| Custom                        | ASM1074 USB30 PORTS  | 10  |
| Date: Tuesday, March 19, 2013 | Sheet 30 of 64       |     |



## FRONT USB30 PORT 0,1



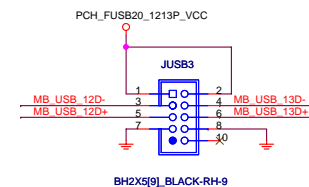
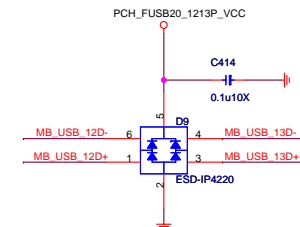
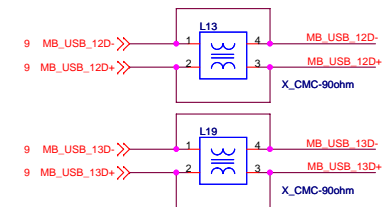
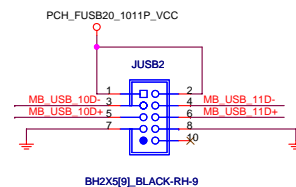
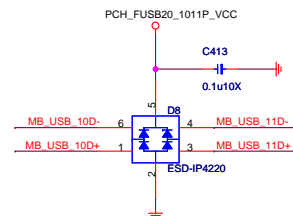
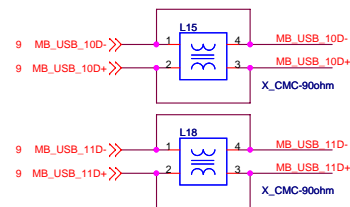
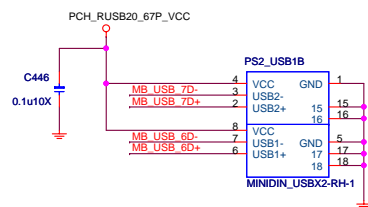
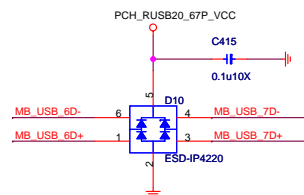
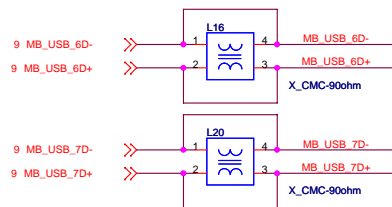
## REAR USB30 PORT 4,5



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| Size                          | Document Description | Rev |
|-------------------------------|----------------------|-----|
| Custom                        | LPT USB30 PORTS      | 10  |
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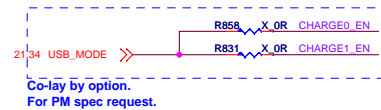
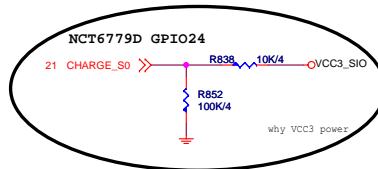
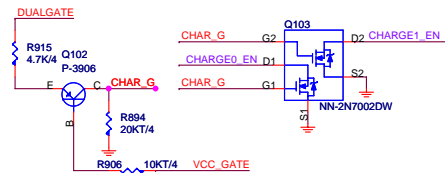


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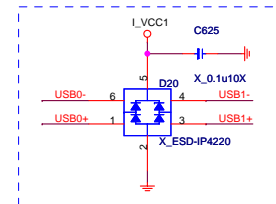
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|-------------------------------|----------------------|-----|
| Custom                        | LPT USB20 PORTS      | 10  |
| Date: Tuesday, March 19, 2013 | Sheet 32 of 64       |     |



[illegible]

Co-lay by option. For PM spec request.



SLG55583A has internal ESD diode.

[illegible]

MAX1.7A

I\_VCC2

EC50  
CD100u16SC

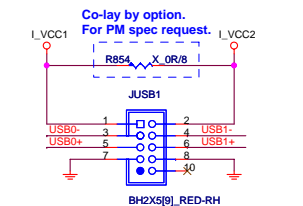
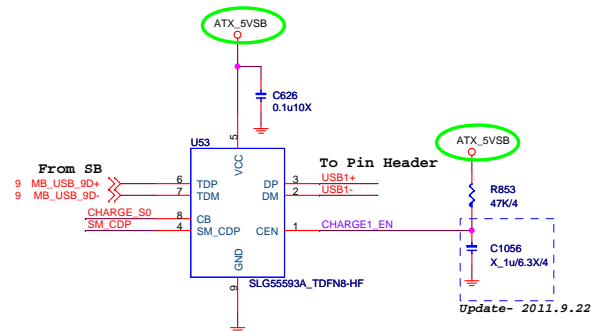
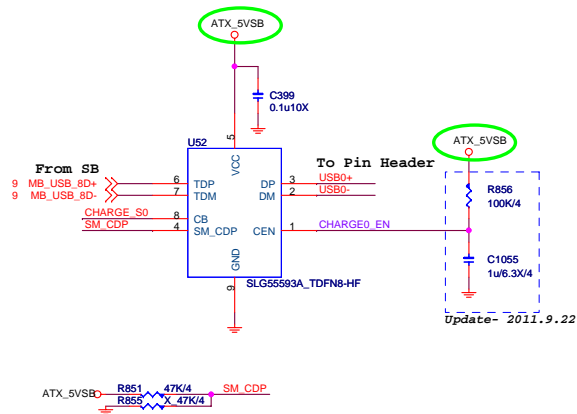
C392  
X.0.1u10X

U24  
UP7534ARA8-15\_MSOP8-PHF

CHARGE1\_EN 4 EN VOUT1 8  
5VDUAL\_USB 2 VIN1 VOUT2 7  
CHARGE\_OC# 5 VIN2 VOUT3 6  
OC#4 4 OC# 1  
GND 1

R863 OR

10,56



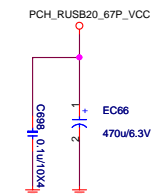
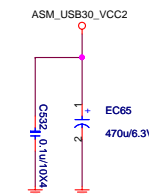
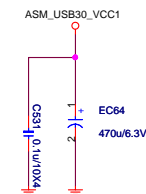
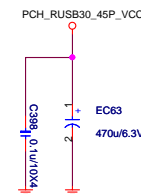
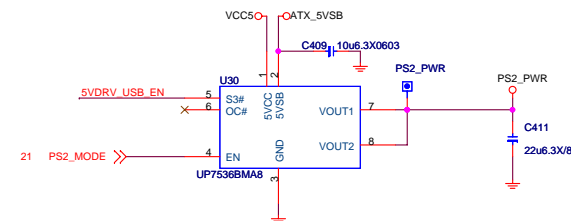
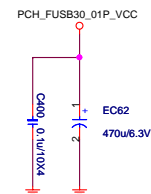
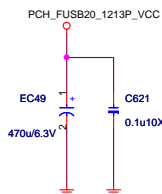
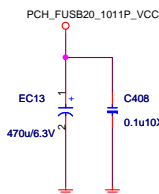
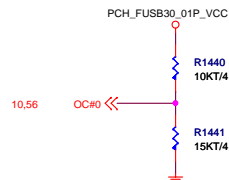
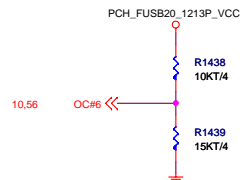
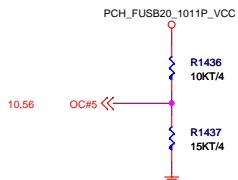
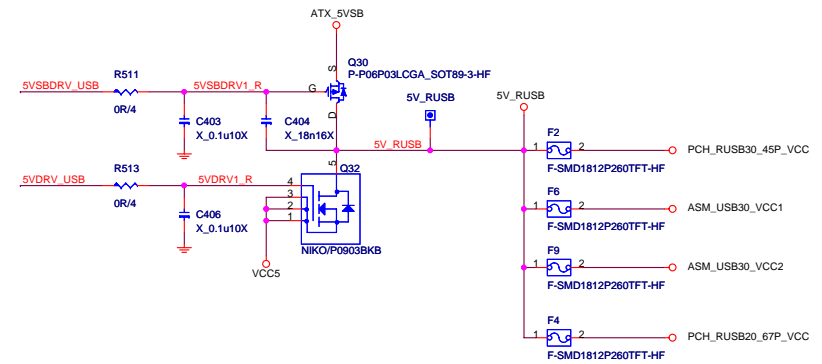
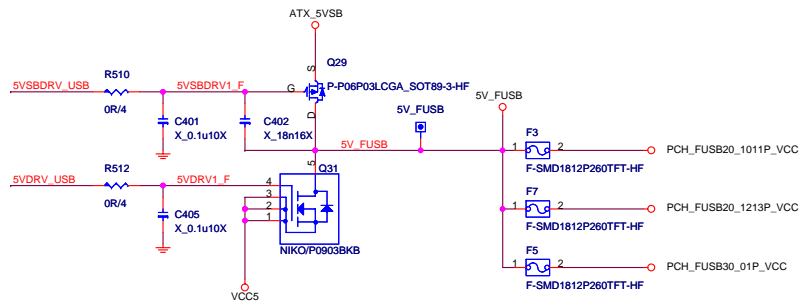
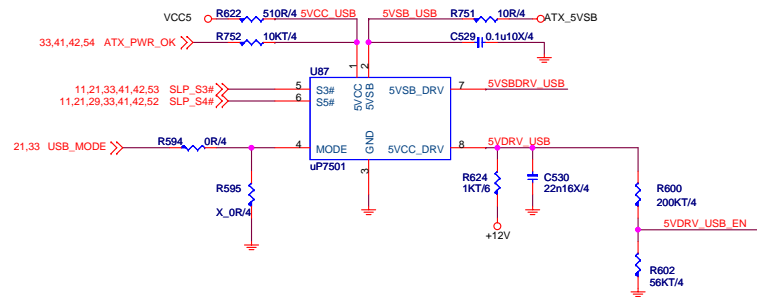
N32-2051A21-H06 Red with Housing

Please name the pin header JUSB1.



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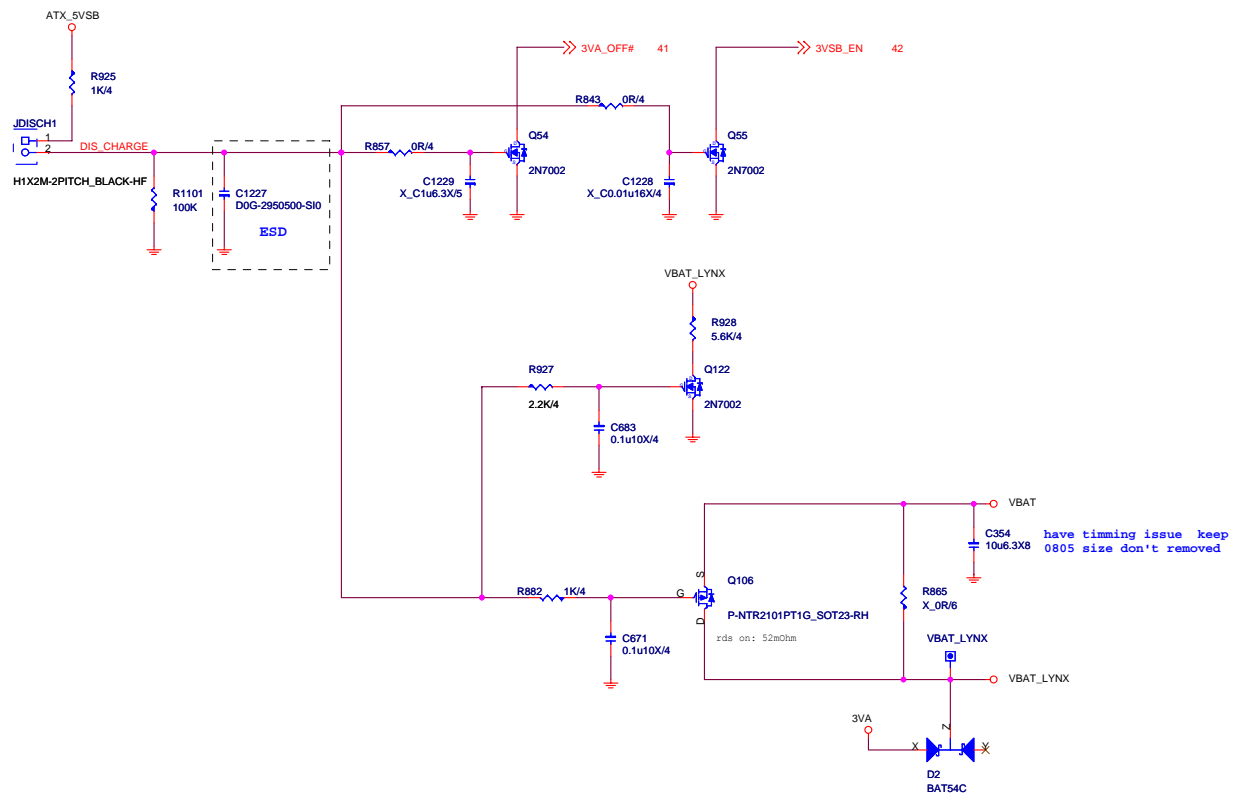
|                               |                                                 |                |
|-------------------------------|-------------------------------------------------|----------------|
| Size<br>Custom                | Document Description<br><b>USB CHARGE PORTS</b> | Rev<br>10      |
| Date: Tuesday, March 19, 2013 |                                                 | Sheet 33 of 64 |



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|        |                                  |                |
|--------|----------------------------------|----------------|
| Size   | Document Description             | Rev            |
| Custom | <b>USB &amp; PS/2 PORT POWER</b> | 10             |
| Date:  | Tuesday, March 19, 2013          | Sheet 34 of 64 |

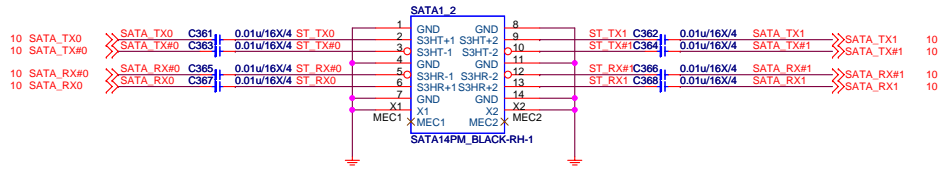


MICRO-STAR INT'L CO.,LTD

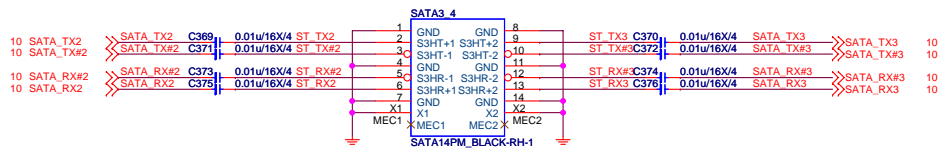
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|                               |                                          |           |
|-------------------------------|------------------------------------------|-----------|
| Size<br>Custom                | Document Description<br><b>DISCHARGE</b> | Rev<br>10 |
| Date: Tuesday, March 19, 2013 | Sheet 35 of 64                           |           |

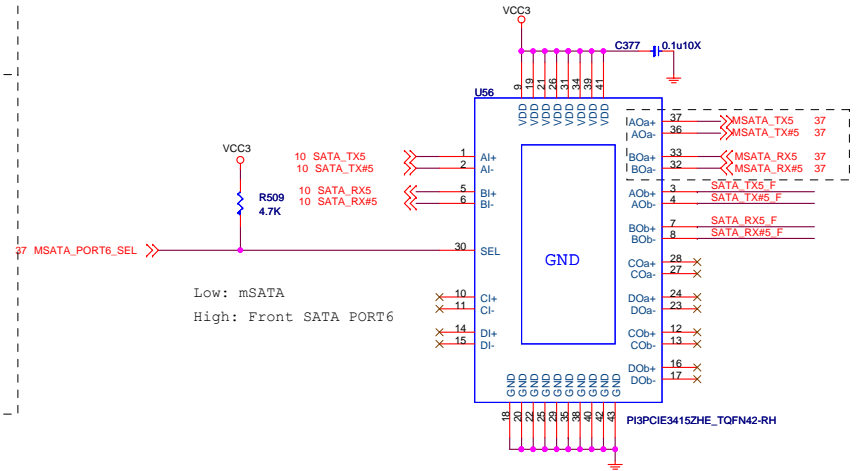
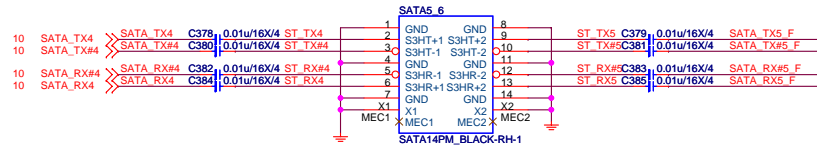
# SATA1-2

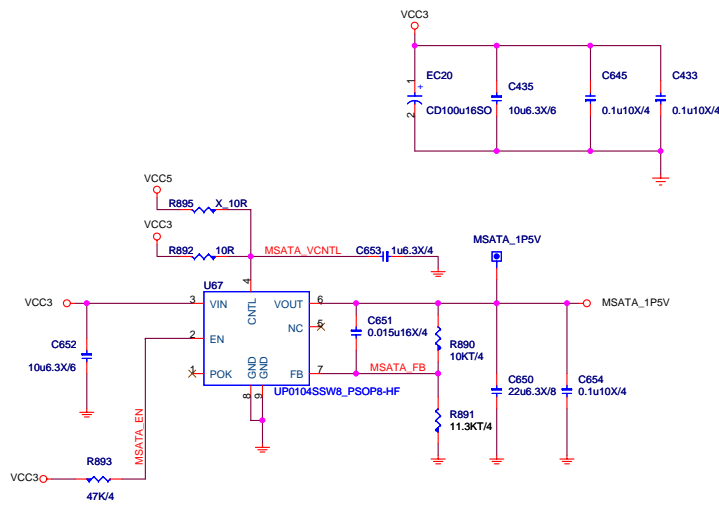


# SATA3-4



# SATA5-6





infect ,miniPCIe ,pin 23 25 need connect to host RX  
infect ,miniPCIe ,pin 31 33 need connect to host TX pin23 for MSATA-  
pin25 for MSATA-

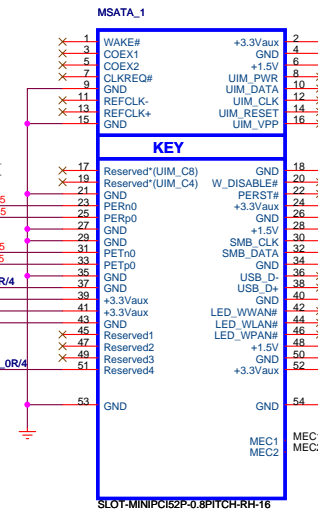
36 MSATA\_RX5 <<< C430 0.01u/16X/4 MSATA\_RXP5  
36 MSATA\_RX#5 <<< C431 0.01u/16X/4 MSATA\_RXN5

36 MSATA\_TX#5 <<< C434 0.01u/16X/4 MSATA\_TXN5  
36 MSATA\_TX5 <<< C436 0.01u/16X/4 MSATA\_TXP5

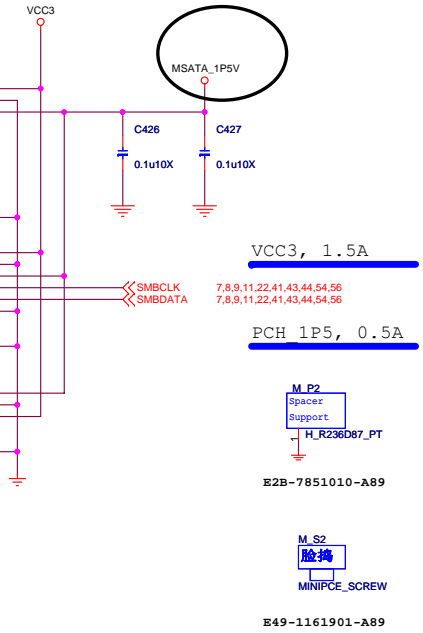
36 MSATA\_PORT6\_SEL <<< R575 0R/4

10.56 PCH\_GPIO49 <<< R576 0R/4

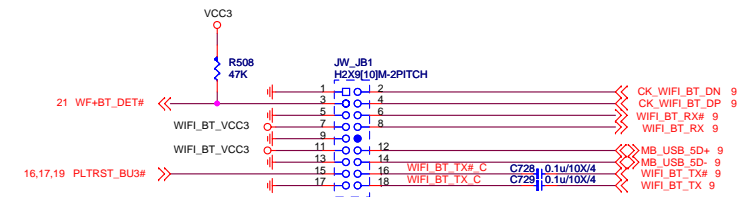
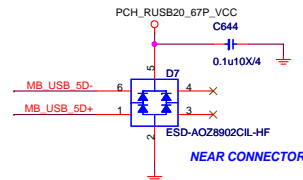
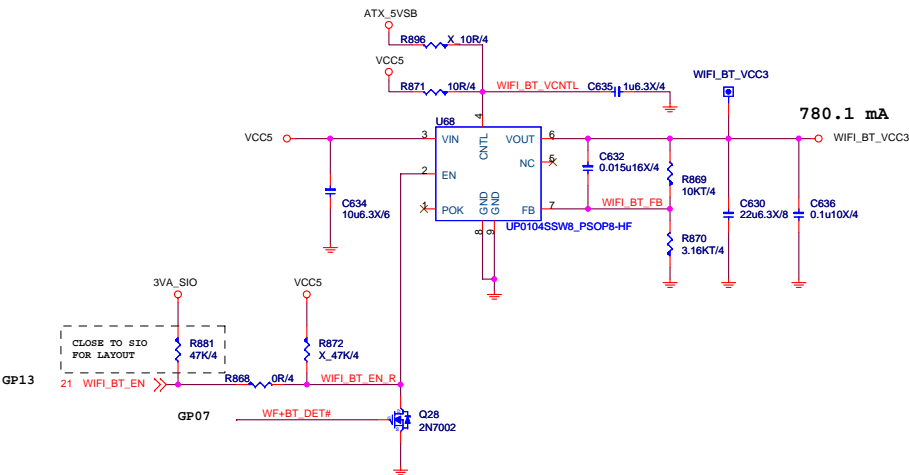
Low: mSATA  
High: Front SATA PORT6



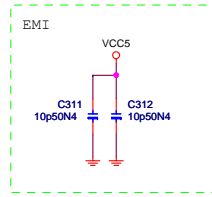
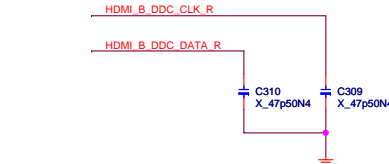
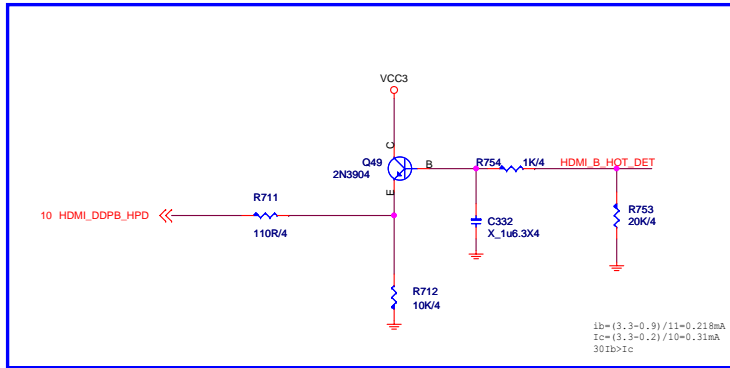
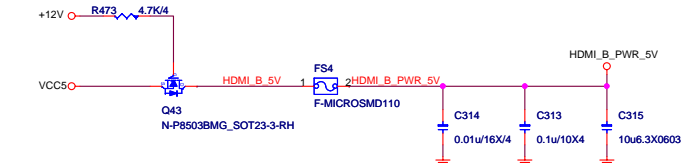
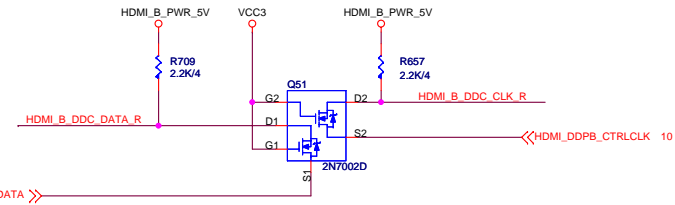
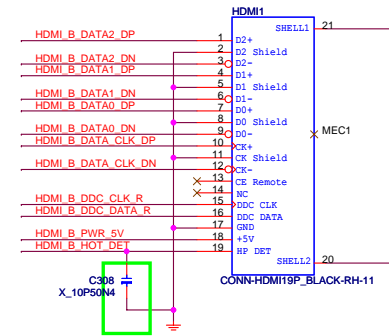
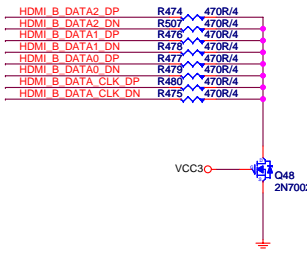
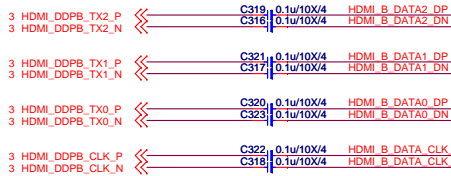
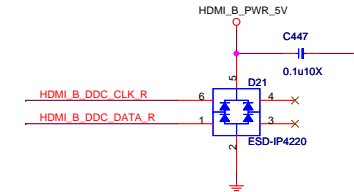
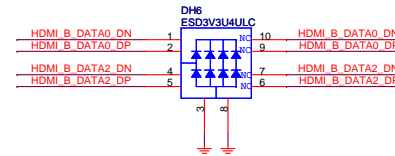
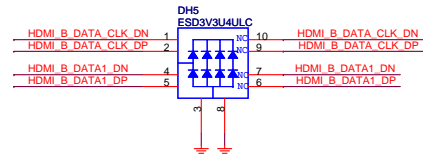
msATA support only



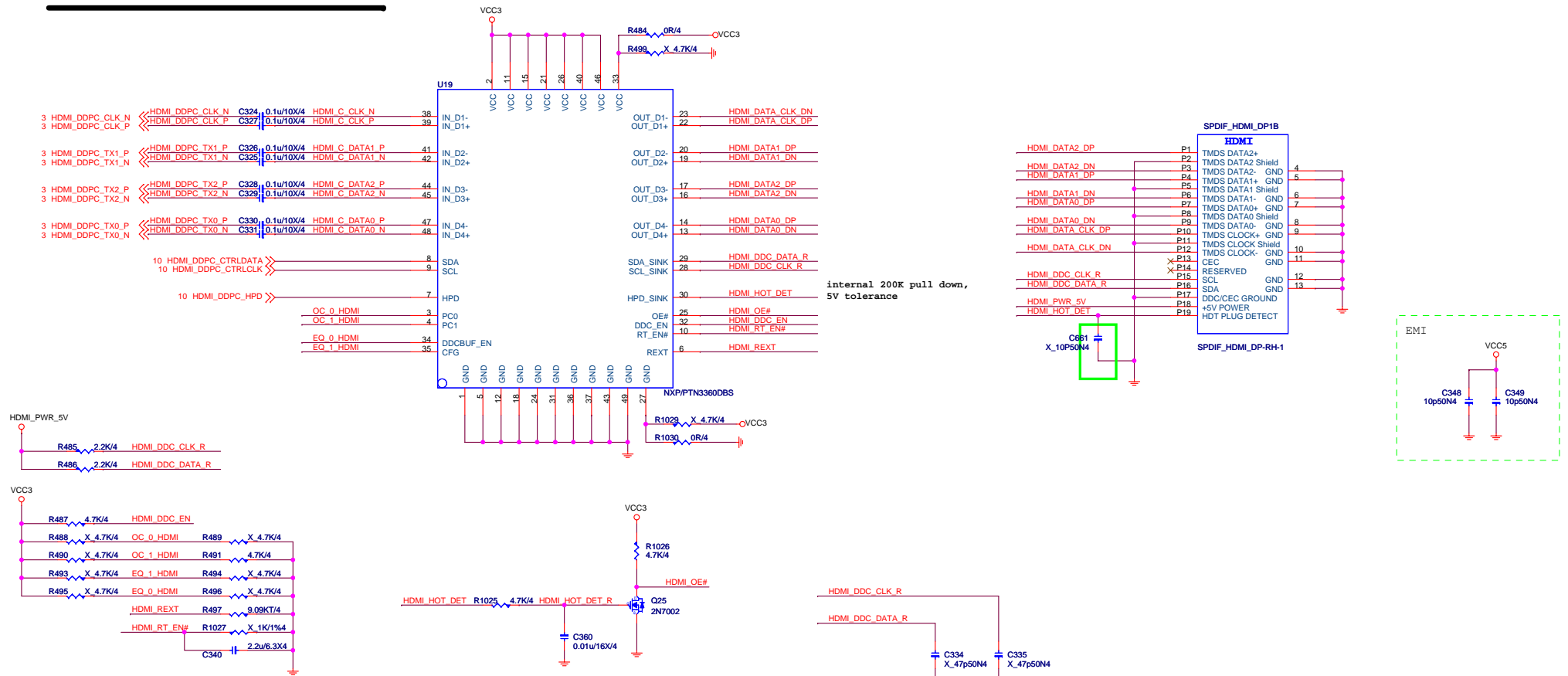
PCI Express  
Mini Card Electromechanical  
Specification  
Revision 1.2



# HDMI level shifter



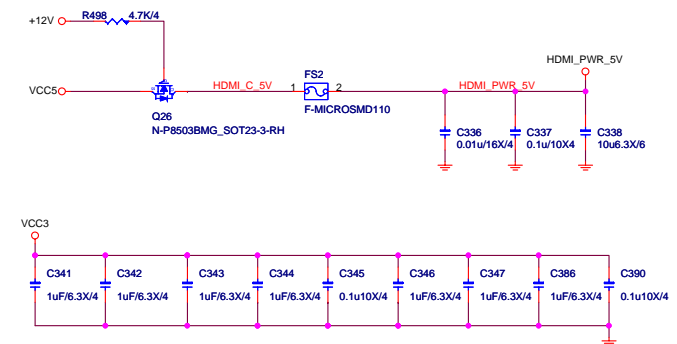
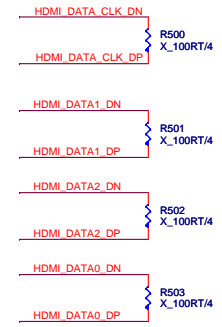
# HDMI level shifter




|           | "0"                                                          | "1"                                                                               | note                                          |
|-----------|--------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------|
| DDC_EN    | DDC level shifter disable                                    | DDC level shifter enable                                                          | internal pull-up at ~500K ohm.                |
| RT_EN#    | Input 50 ohm termination resistor enable                     | the input termination ; resistors are set to high impedances                      | internal pull-down at ~500K ohm.              |
| OE#       | enable                                                       | the chip is power down and input termination resistors will be at high impedance. | internal pull-down at ~500K ohm.              |
| HPD_SINK  | disable                                                      | enable                                                                            | internal pull-down at ~200K ohm.              |
| DDCBUF_EN | For DDC level shifting configuration, please refer to Table. |                                                                                   | 5V tolerant, internal pull-down at ~500K ohm. |
| REXT      |                                                              |                                                                                   | analog current generation.                    |

| [DDC_EN, DDCBUF_EN, OE#] | DDC Passive Switch | DDC Active Buffer | PCI, PC0 | note  |
|--------------------------|--------------------|-------------------|----------|-------|
| 1, 0, X                  | On                 | Off               | 00       | 8 dB  |
| 1, 1, 0                  | Off                | On                | 01       | 4 dB  |
| 1, 1, 1                  | Off                | Off               | 10       | 12 dB |
| 0, X, X                  | Off                | Off               | 11       | 0 dB  |

EMI





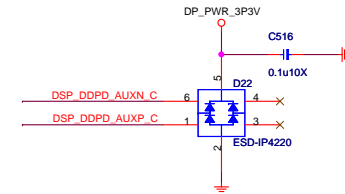
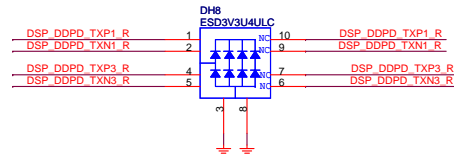
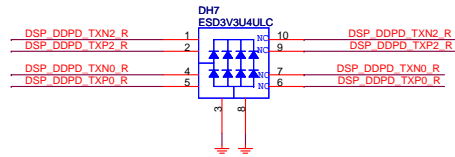
**MSI**

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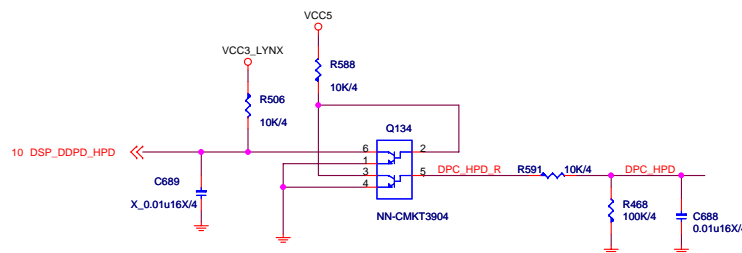
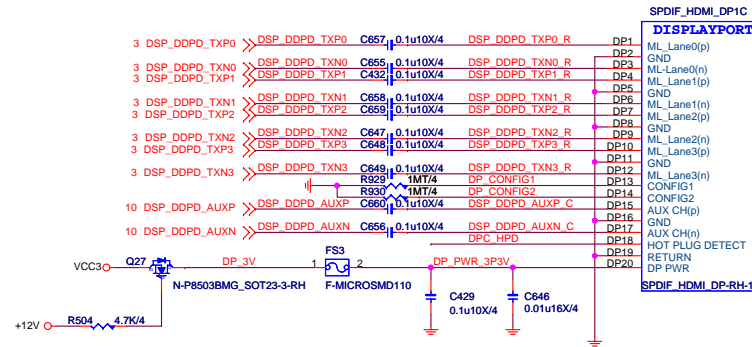
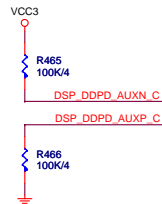
**MS-7818**

Size Custom Document Description  
**HDMI PORT C**

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## DP



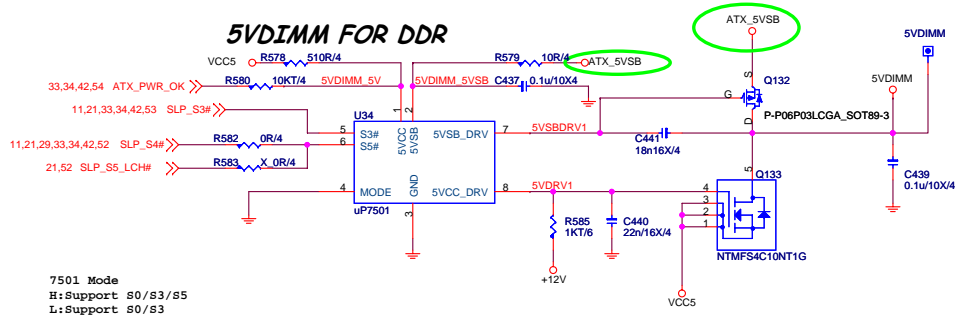
MICRO-STAR INT'L CO.,LTD

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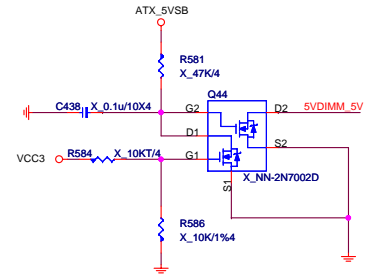
|       |                         |                      |          |
|-------|-------------------------|----------------------|----------|
| Size  | Custom                  | Document Description | Rev      |
|       |                         | DISPLAY PORT D       | 10       |
| Date: | Tuesday, March 19, 2013 | Sheet                | 40 of 64 |



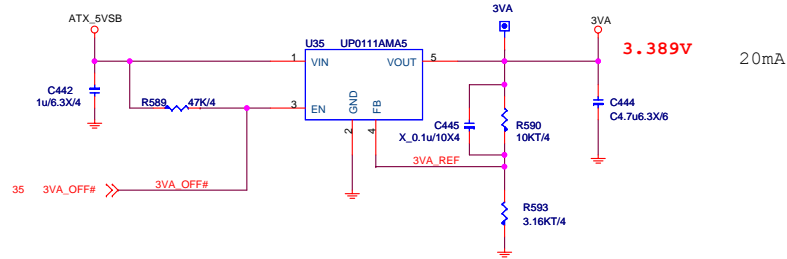
## 5VDIMM FOR DDR



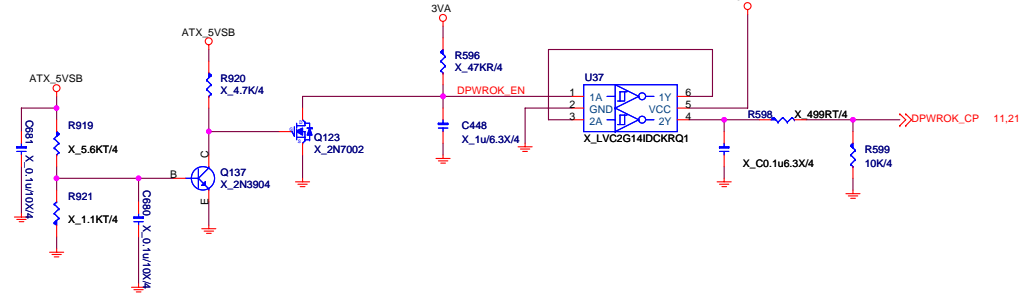
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.



## 3VA

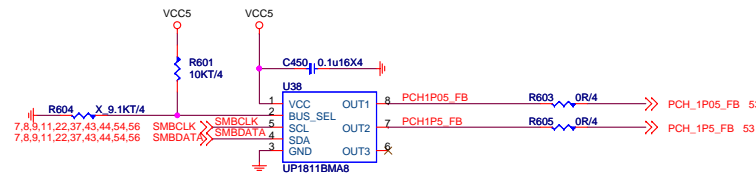


FOR DPWROK and 3VA sequence (S5-->G3-->S5)



## UPI VOLTAGE CONSOLE

| 0x20: RH=1.0K, RL=OPEN |      |      |      |      |      |      |
|------------------------|------|------|------|------|------|------|
| ADDRESS                | 0x2A | 0x28 | 0x26 | 0x24 | 0x22 | 0x20 |
| RH (KOhm)              | OPEN | 3.9  | 3    | 2.2  | 1.3  | 10   |
| RL (KOhm)              | 10   | 1.3  | 2.3  | 3    | 3.9  | OPEN |
| BUS_SEL                | 0%   | 25%  | 40%  | 60%  | 75%  | 100% |

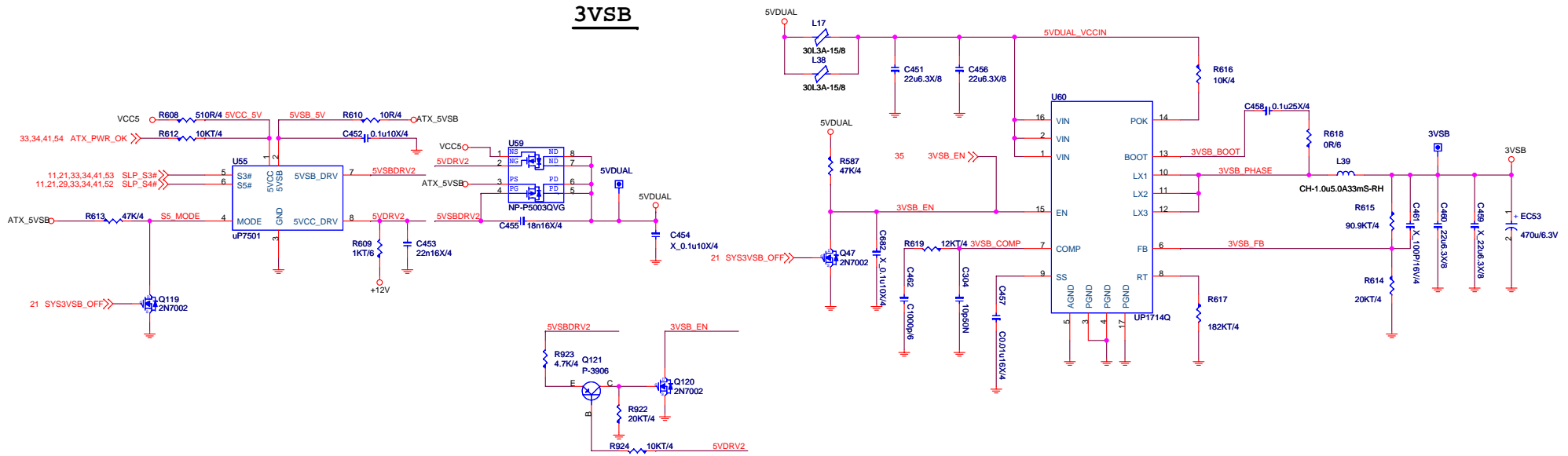


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|-------------------------------|----------------------|-----|
| Custom                        | ACPI PARTI           | 10  |
| Date: Tuesday, March 19, 2013 | Sheet 41 of 64       |     |

3VSB



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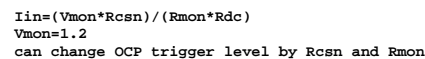
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| Size | Custom |
|------|--------|

|                      |
|----------------------|
| Document Description |
| <b>ACPI PART2</b>    |

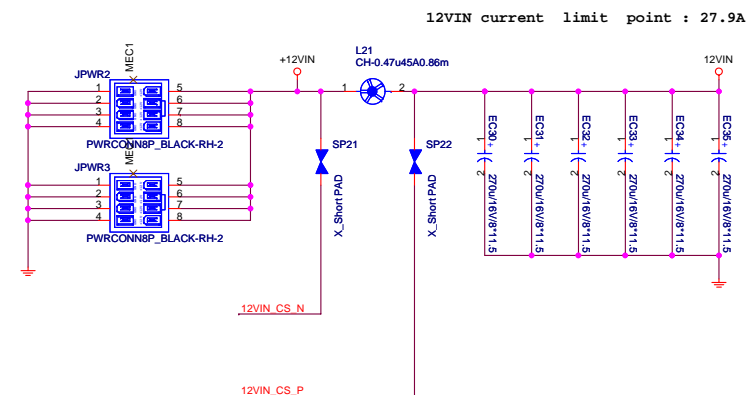
Date: T

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0x2A: RH=OPEN, RL=10K

[illegible]

0xD4:RL=10K

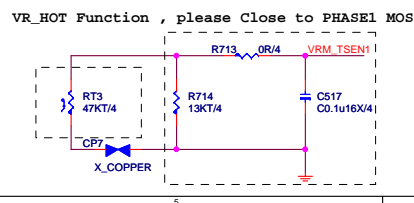
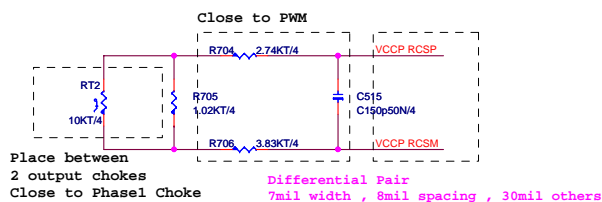
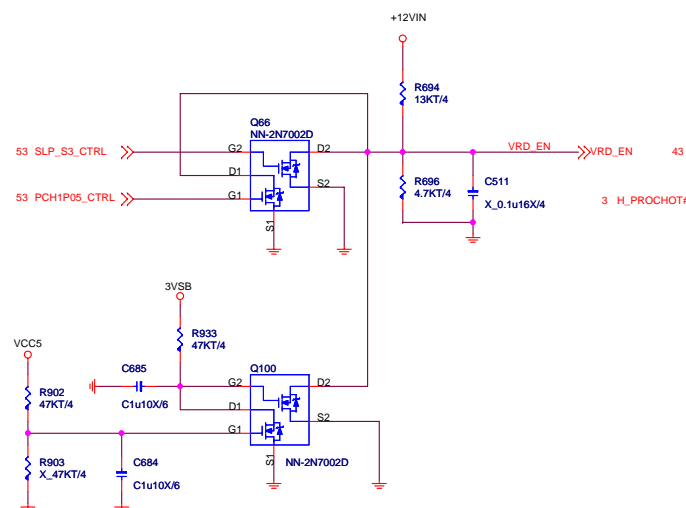
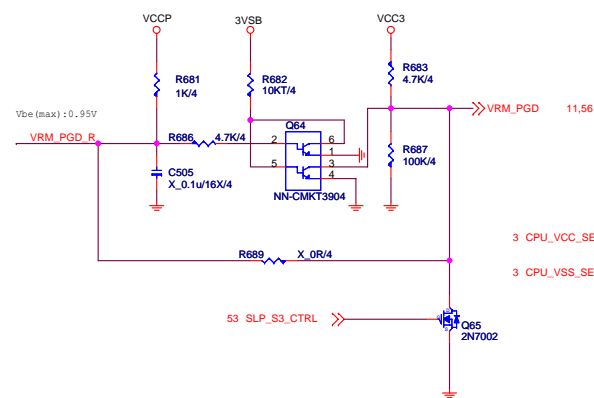
[illegible]

**MS-7818**

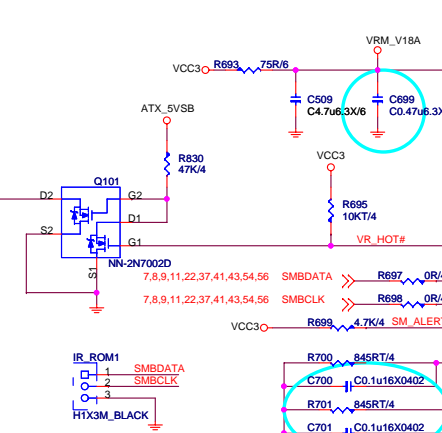
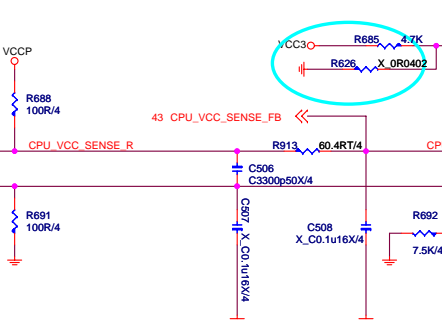
|     |    |
|-----|----|
| Rev | 10 |
|-----|----|

|                               |                |
|-------------------------------|----------------|
| Date: Tuesday, March 19, 2013 | Sheet 43 of 64 |
|-------------------------------|----------------|

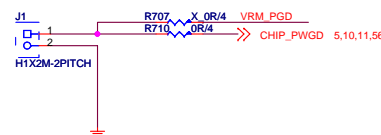
## VRMPWRGD LEVEL SHIFT



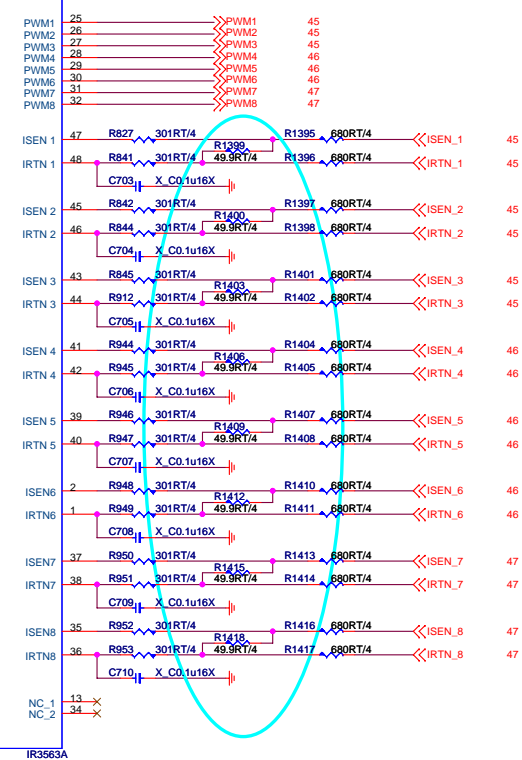
close to VRM



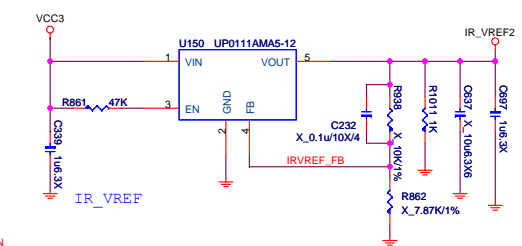
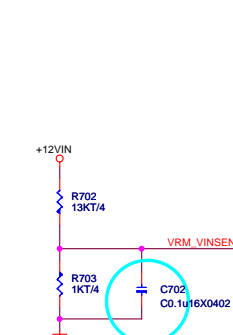
```
ADDR_PROT: Stuff 845 ohm for SMBUS Address 0X70 use
SV ADDR: Stuff 845 ohm for SVID Address 0 use
```



BOTTOM PAD  
CONNECT TO GND  
Through 8 VIAs



1.2V

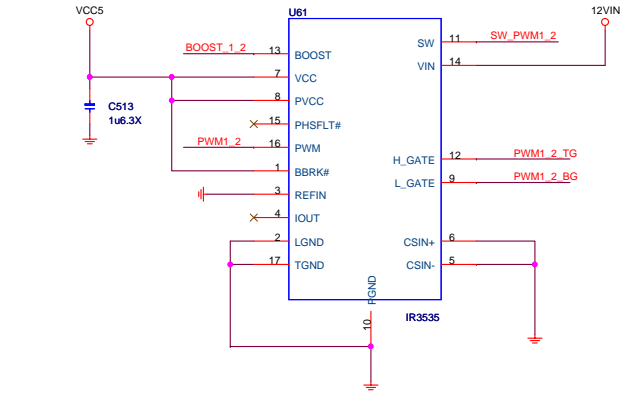
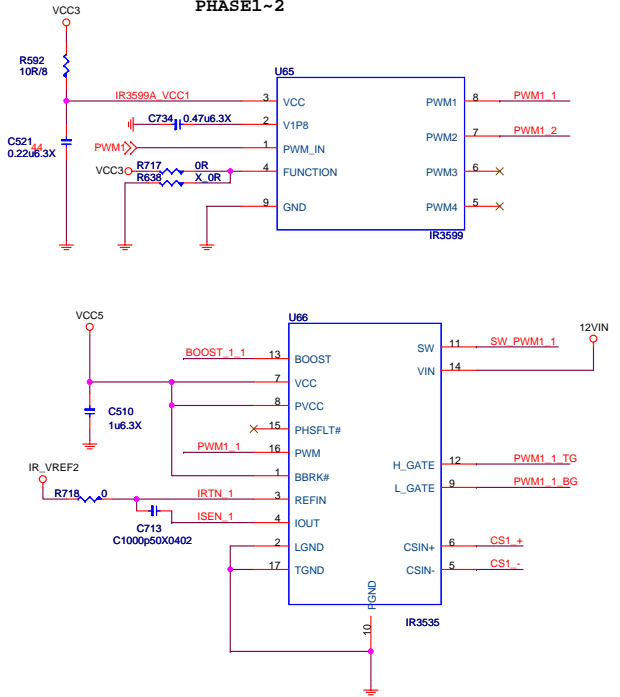


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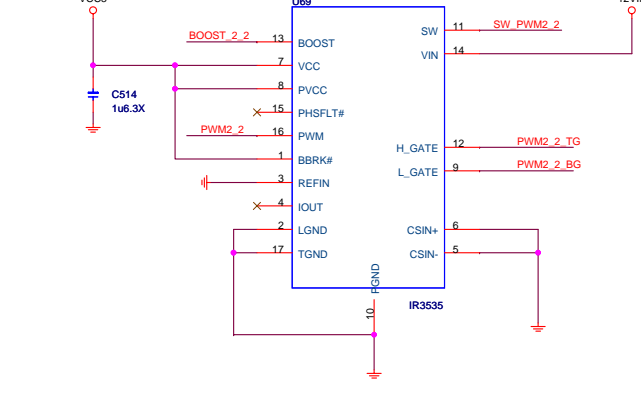
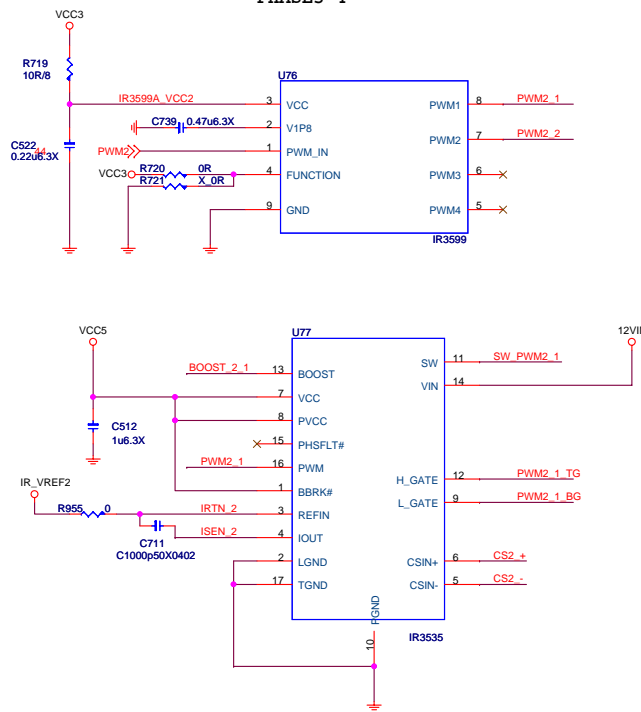
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| Date: Tuesday, March 19, 2013 |                                                      | Sheet 44 of 64 |

# PHASE1~2



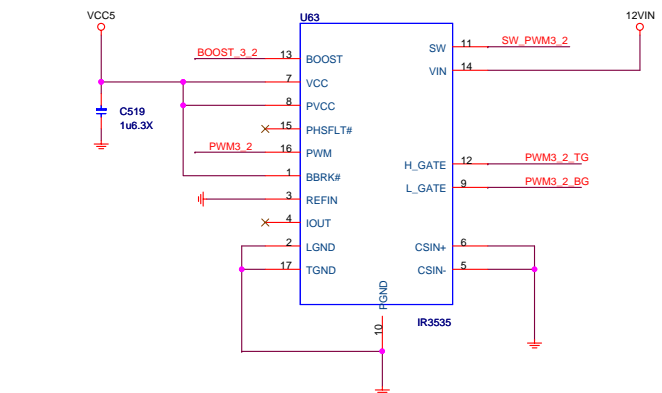
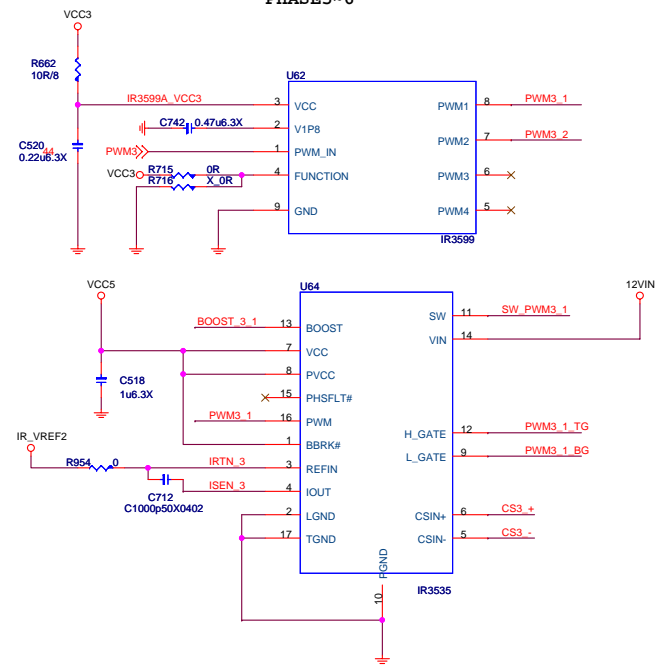
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|-----------|-----------|----|-----------|-----------|----|--------|--------|----|
| SW_PWM1_1 | SW_PWM1_1 | 48 | PWM1_1_TG | PWM1_1_TG | 48 | IRTN_1 | IRTN_1 | 44 |
| SW_PWM1_2 | SW_PWM1_2 | 48 | PWM1_1_BG | PWM1_1_BG | 48 | ISEN_1 | ISEN_1 | 44 |
| BOOST_1_1 | BOOST_1_1 | 48 | PWM1_2_TG | PWM1_2_TG | 48 | CS1_+  | CS1_+  | 48 |
| BOOST_1_2 | BOOST_1_2 | 48 | PWM1_2_BG | PWM1_2_BG | 48 | CS1_-  | CS1_-  | 48 |

# PHASE3~4



|           |           |    |           |           |    |        |        |    |
|-----------|-----------|----|-----------|-----------|----|--------|--------|----|
| SW_PWM2_1 | SW_PWM2_1 | 48 | PWM2_1_TG | PWM2_1_TG | 48 | IRTN_2 | IRTN_2 | 44 |
| SW_PWM2_2 | SW_PWM2_2 | 48 | PWM2_1_BG | PWM2_1_BG | 48 | ISEN_2 | ISEN_2 | 44 |
| BOOST_2_1 | BOOST_2_1 | 48 | PWM2_2_TG | PWM2_2_TG | 48 | CS2_+  | CS2_+  | 48 |
| BOOST_2_2 | BOOST_2_2 | 48 | PWM2_2_BG | PWM2_2_BG | 48 | CS2_-  | CS2_-  | 48 |

# PHASE5~6



|           |           |    |           |           |    |        |        |    |
|-----------|-----------|----|-----------|-----------|----|--------|--------|----|
| SW_PWM3_1 | SW_PWM3_1 | 49 | PWM3_1_TG | PWM3_1_TG | 49 | IRTN_3 | IRTN_3 | 44 |
| SW_PWM3_2 | SW_PWM3_2 | 49 | PWM3_1_BG | PWM3_1_BG | 49 | ISEN_3 | ISEN_3 | 44 |
| BOOST_3_1 | BOOST_3_1 | 49 | PWM3_2_TG | PWM3_2_TG | 49 | CS3_+  | CS3_+  | 49 |
| BOOST_3_2 | BOOST_3_2 | 49 | PWM3_2_BG | PWM3_2_BG | 49 | CS3_-  | CS3_-  | 49 |

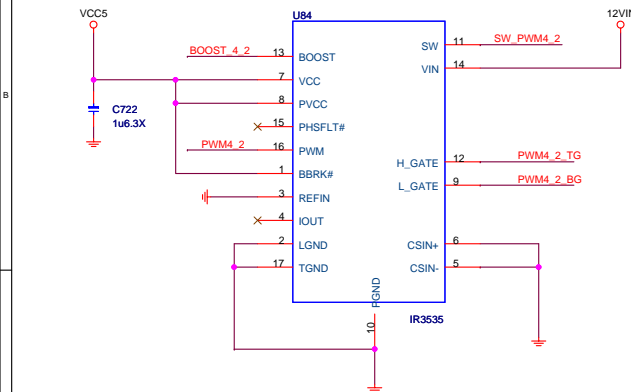
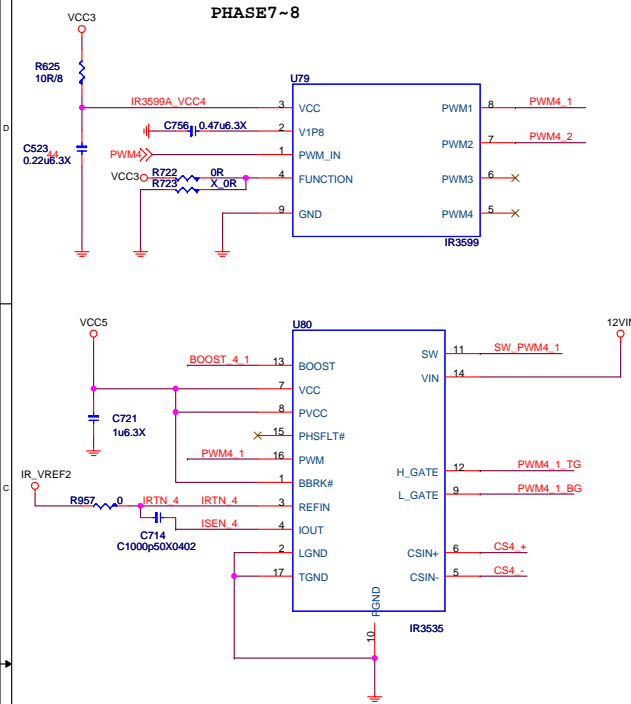


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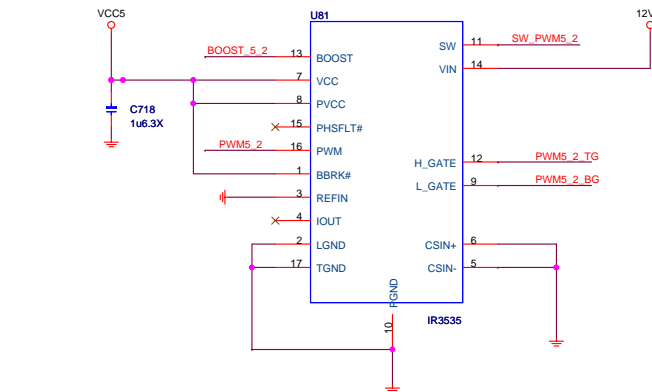
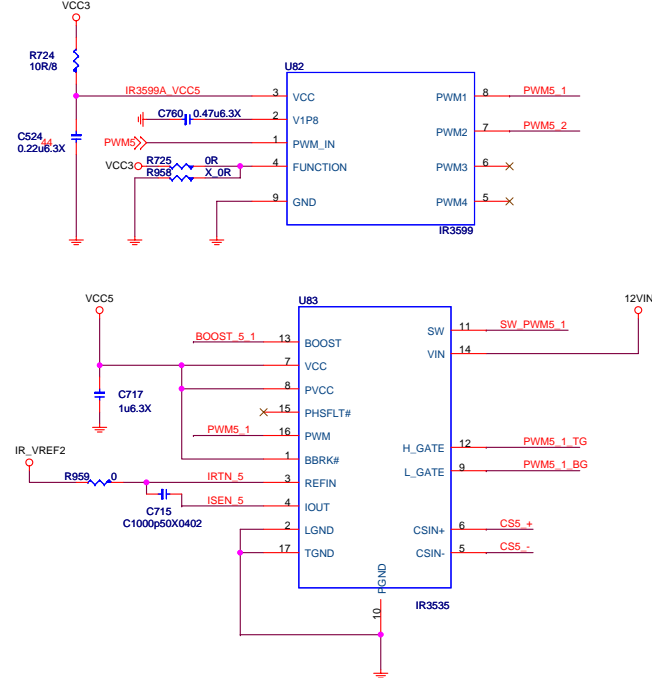
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| Size   | Document Description                | Rev            |
| Custom | <b>VCORE IR3599-IR3535 PHASE1-6</b> | 10             |
| Date:  | Tuesday, March 19, 2013             | Sheet 45 of 64 |

# PHASE7~8



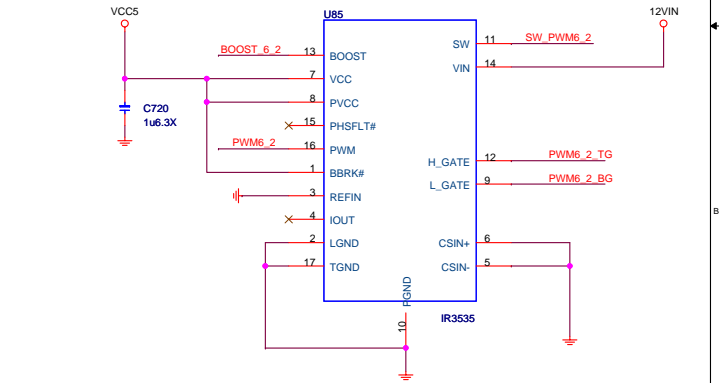
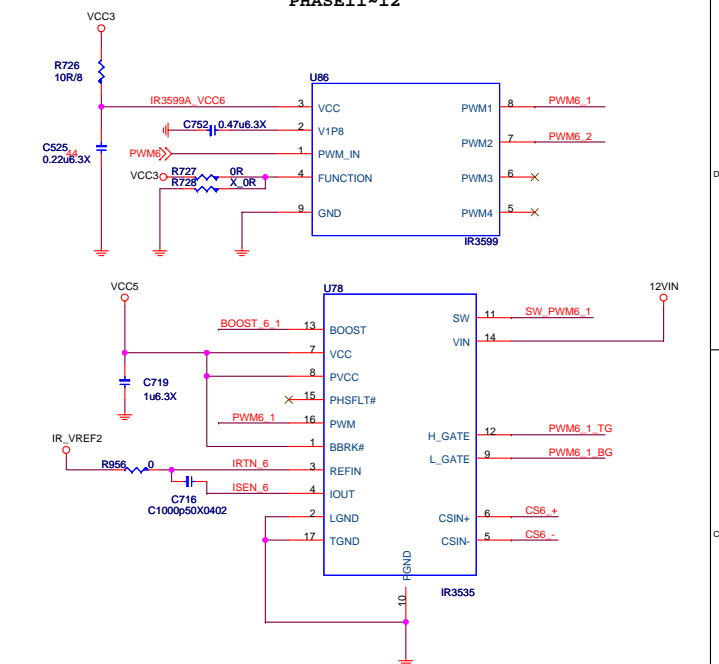
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|-----------|-----------|----|-----------|-----------|----|--------|--------|----|
| SW_PWM4_1 | SW_PWM4_1 | 49 | PWM4_1_TG | PWM4_1_TG | 49 | IRTN_4 | IRTN_4 | 44 |
| SW_PWM4_2 | SW_PWM4_2 | 49 | PWM4_1_BG | PWM4_1_BG | 49 | ISEN_4 | ISEN_4 | 44 |
| BOOST_4_1 | BOOST_4_1 | 49 | PWM4_2_TG | PWM4_2_TG | 49 | CS4_+  | CS4_+  | 49 |
| BOOST_4_2 | BOOST_4_2 | 49 | PWM4_2_BG | PWM4_2_BG | 49 | CS4_-  | CS4_-  | 49 |

# PHASE9~10



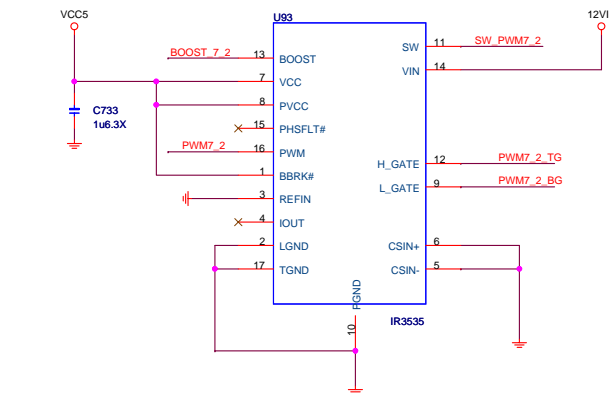
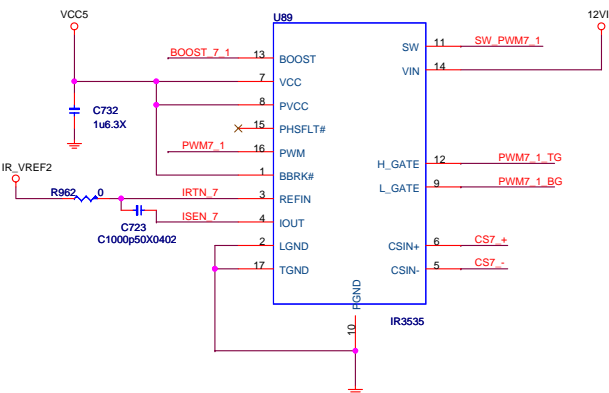
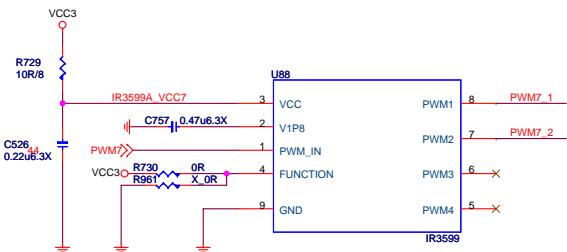
|           |           |    |           |           |    |        |        |    |
|-----------|-----------|----|-----------|-----------|----|--------|--------|----|
| SW_PWM5_1 | SW_PWM5_1 | 50 | PWM5_1_TG | PWM5_1_TG | 50 | IRTN_5 | IRTN_5 | 44 |
| SW_PWM5_2 | SW_PWM5_2 | 50 | PWM5_1_BG | PWM5_1_BG | 50 | ISEN_5 | ISEN_5 | 44 |
| BOOST_5_1 | BOOST_5_1 | 50 | PWM5_2_TG | PWM5_2_TG | 50 | CS5_+  | CS5_+  | 50 |
| BOOST_5_2 | BOOST_5_2 | 50 | PWM5_2_BG | PWM5_2_BG | 50 | CS5_-  | CS5_-  | 50 |

# PHASE11~12



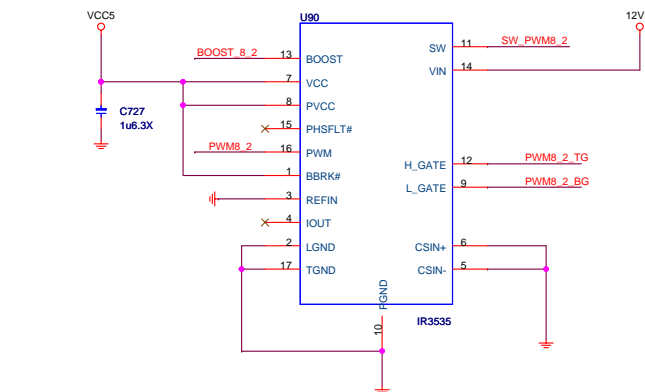
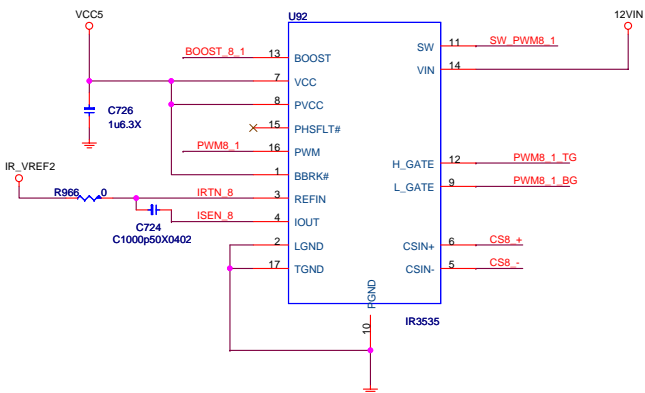
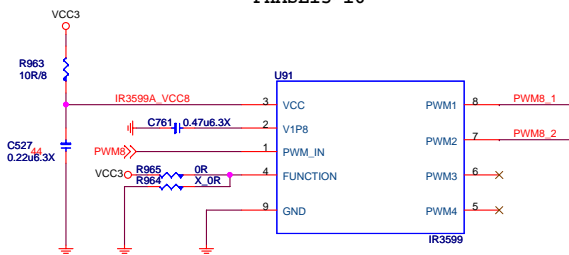
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|-----------|-----------|----|-----------|-----------|----|--------|--------|----|
| SW_PWM6_1 | SW_PWM6_1 | 50 | PWM6_1_TG | PWM6_1_TG | 50 | IRTN_6 | IRTN_6 | 44 |
| SW_PWM6_2 | SW_PWM6_2 | 50 | PWM6_1_BG | PWM6_1_BG | 50 | ISEN_6 | ISEN_6 | 44 |
| BOOST_6_1 | BOOST_6_1 | 50 | PWM6_2_TG | PWM6_2_TG | 50 | CS6_+  | CS6_+  | 50 |
| BOOST_6_2 | BOOST_6_2 | 50 | PWM6_2_BG | PWM6_2_BG | 50 | CS6_-  | CS6_-  | 50 |

# PHASE13~14

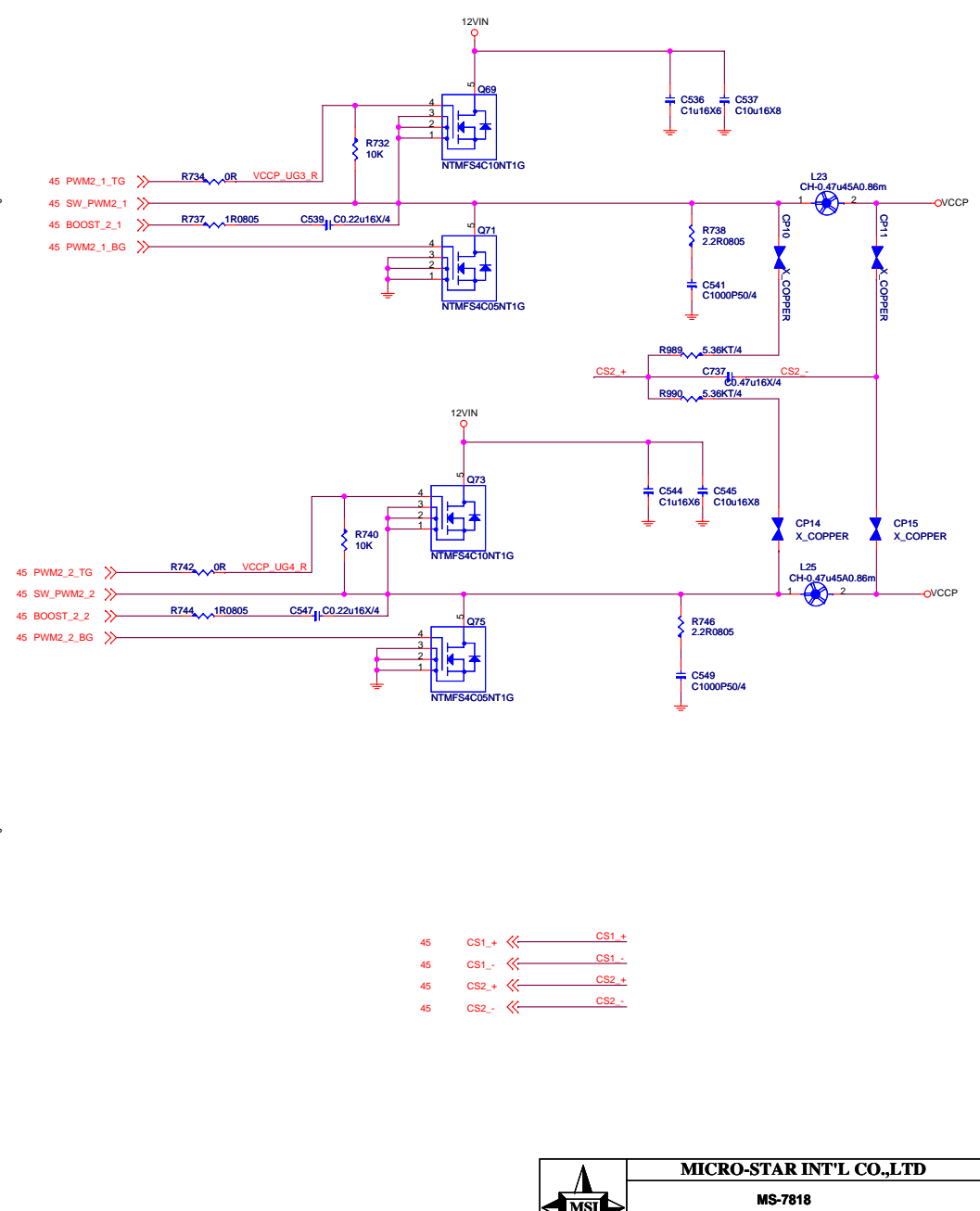
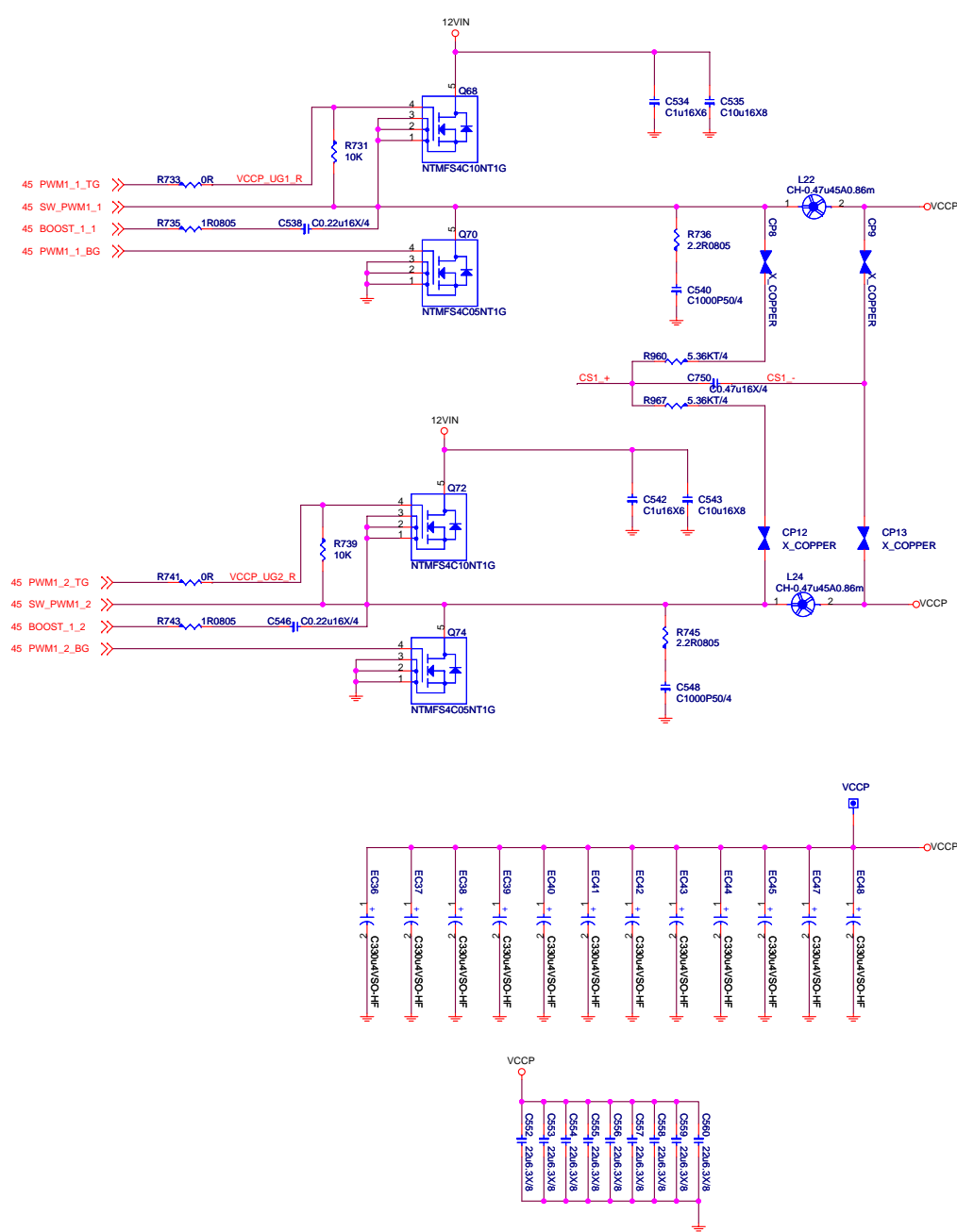


|           |           |    |           |           |    |        |        |    |
|-----------|-----------|----|-----------|-----------|----|--------|--------|----|
| SW_PWM7_1 | SW_PWM7_1 | 51 | PWM7_1_TG | PWM7_1_TG | 51 | IRTN_7 | IRTN_7 | 44 |
| SW_PWM7_2 | SW_PWM7_2 | 51 | PWM7_1_BG | PWM7_1_BG | 51 | ISEN_7 | ISEN_7 | 44 |
| BOOST_7_1 | BOOST_7_1 | 51 | PWM7_2_TG | PWM7_2_TG | 51 | CS7_+  | CS7_+  | 51 |
| BOOST_7_2 | BOOST_7_2 | 51 | PWM7_2_BG | PWM7_2_BG | 51 | CS7_-  | CS7_-  | 51 |

# PHASE15~16

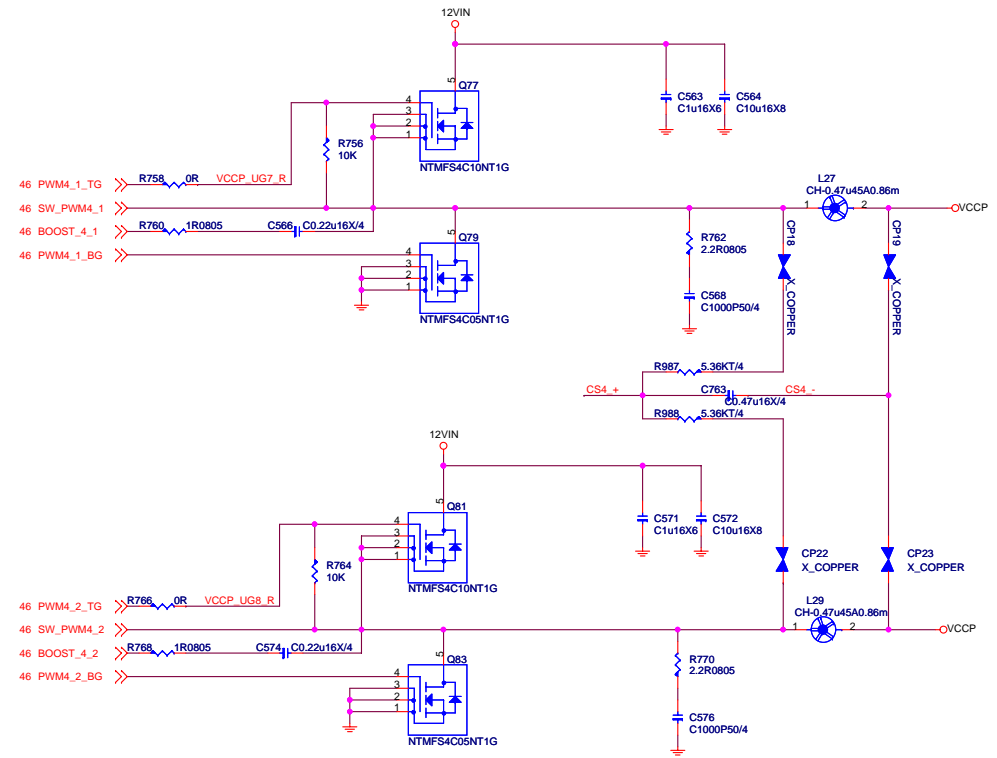
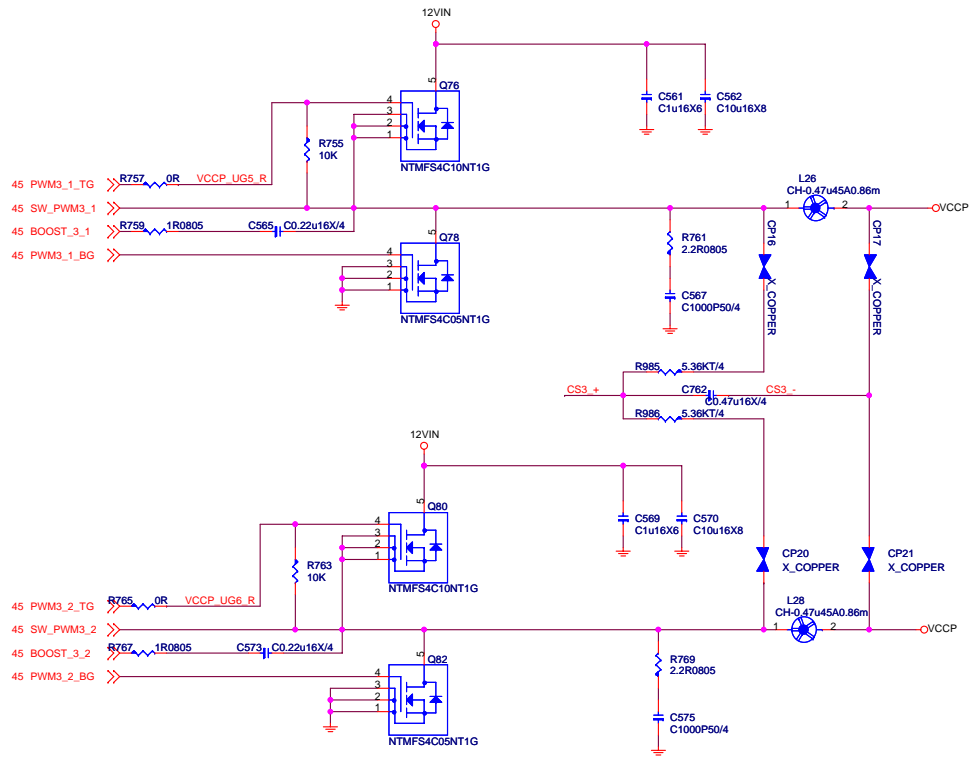


|           |           |    |           |           |    |        |        |    |
|-----------|-----------|----|-----------|-----------|----|--------|--------|----|
| SW_PWM8_1 | SW_PWM8_1 | 51 | PWM8_1_TG | PWM8_1_TG | 51 | IRTN_8 | IRTN_8 | 44 |
| SW_PWM8_2 | SW_PWM8_2 | 51 | PWM8_1_BG | PWM8_1_BG | 51 | ISEN_8 | ISEN_8 | 44 |
| BOOST_8_1 | BOOST_8_1 | 51 | PWM8_2_TG | PWM8_2_TG | 51 | CS8_+  | CS8_+  | 51 |
| BOOST_8_2 | BOOST_8_2 | 51 | PWM8_2_BG | PWM8_2_BG | 51 | CS8_-  | CS8_-  | 51 |



45 CS1\_+ <<< CS1\_+  
 45 CS1\_- <<< CS1\_-  
 45 CS2\_+ <<< CS2\_+  
 45 CS2\_- <<< CS2\_-





45 CS3\_+ << CS3\_+

45 CS3\_- << CS3\_-

46 CS4\_+ << CS4\_+

46 CS4\_- << CS4\_-

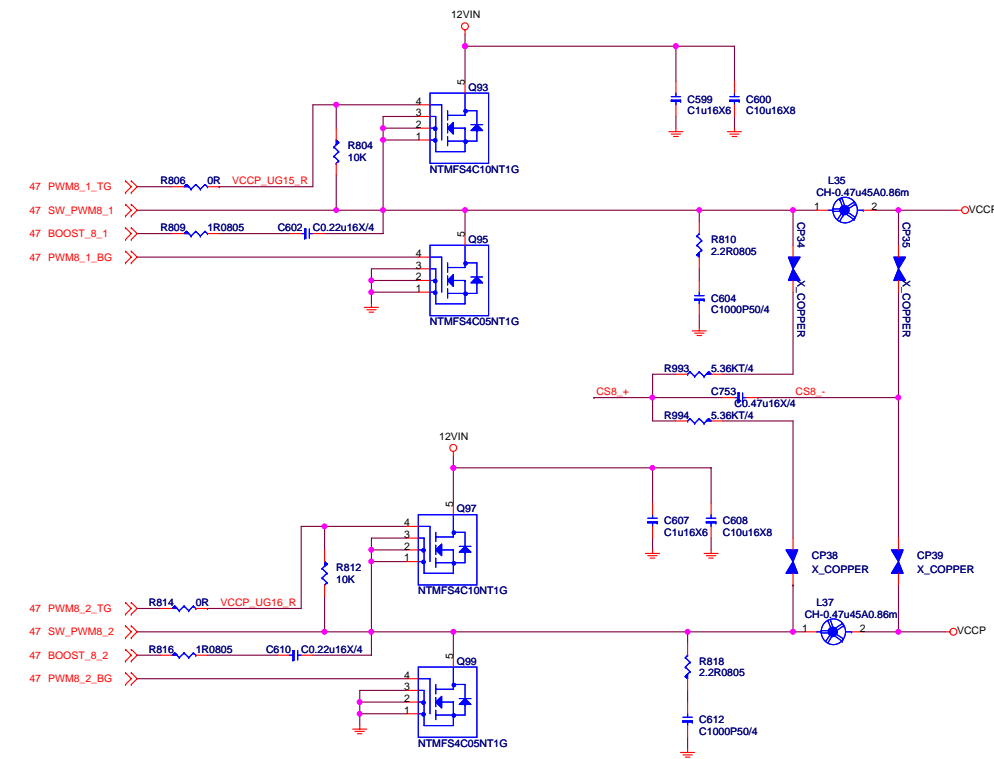
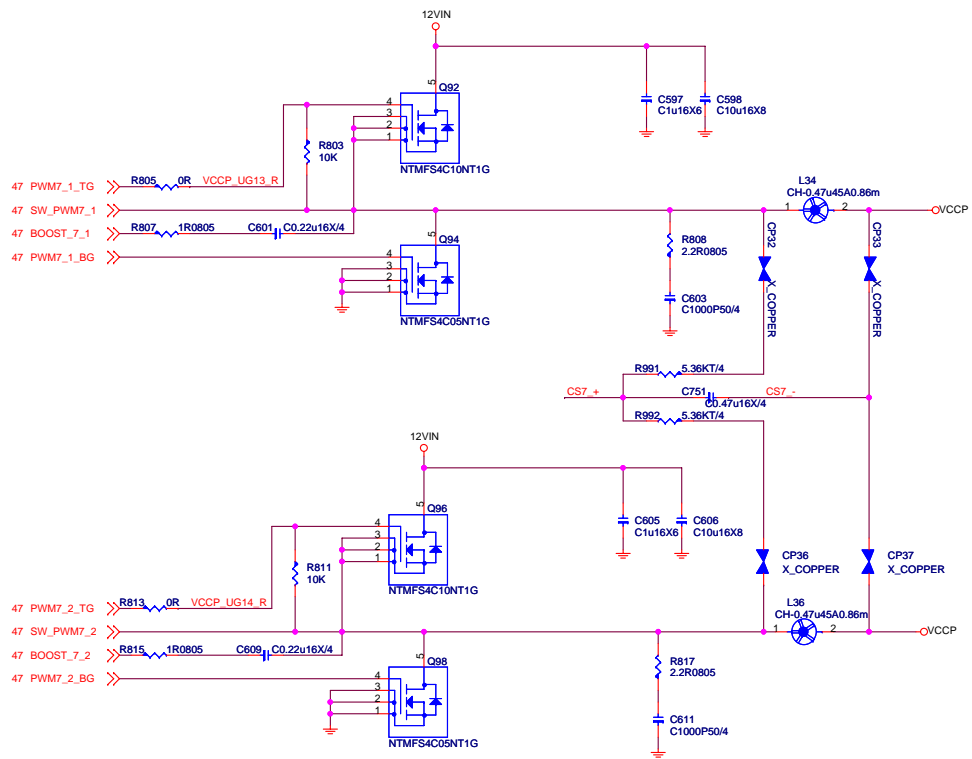


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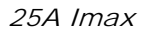
47 CS7\_+ <<< CS7\_+

47 CS7\_- <<< CS7\_-

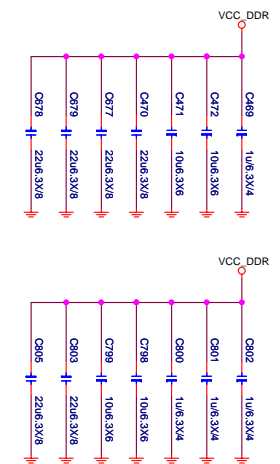
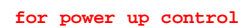
47 CS8\_+ <<< CS8\_+

47 CS8\_- <<< CS8\_-

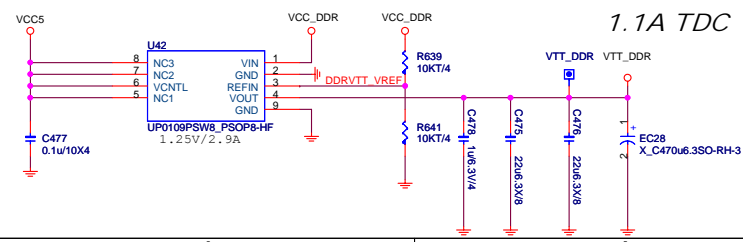
**DDR Power:1.5V**



Place between CPU and DIMMs



### 1.1A TDC



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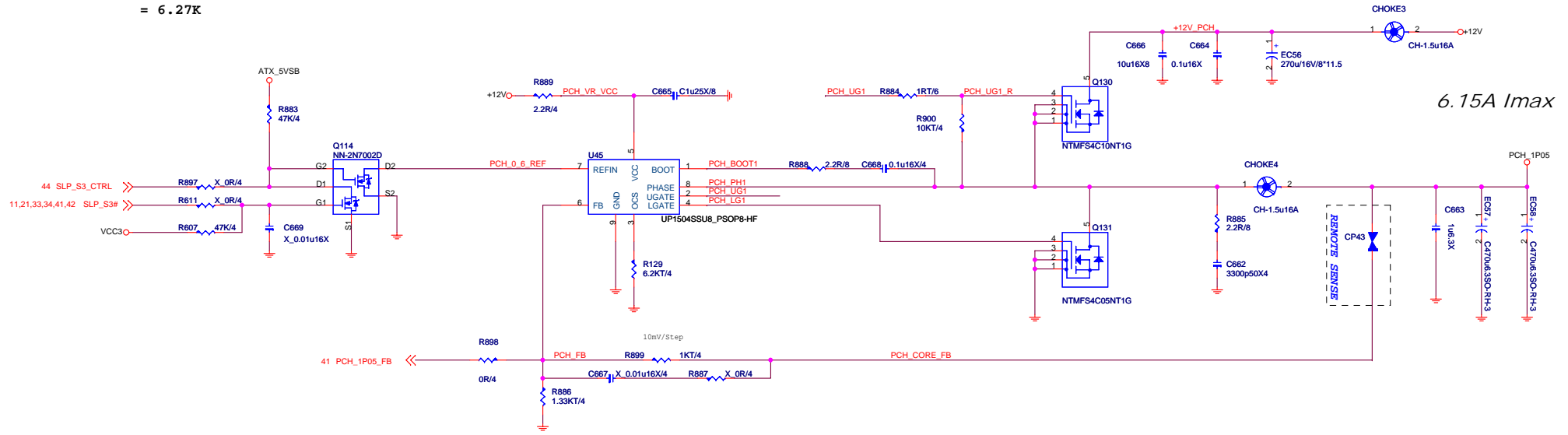
|                               |                |
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$$R_{ocs} = 4 \cdot I_{ocp} \cdot R_{dson} / 20 \mu A$$

$$= 4 \cdot (6.15 \cdot 1.5) \cdot 3.4 m\Omega / 20 \mu A$$

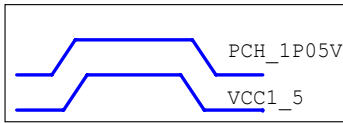
$$= 6.27 K$$

## 1.05V\_PCH

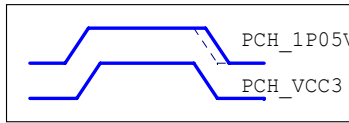


6.15A I<sub>max</sub>

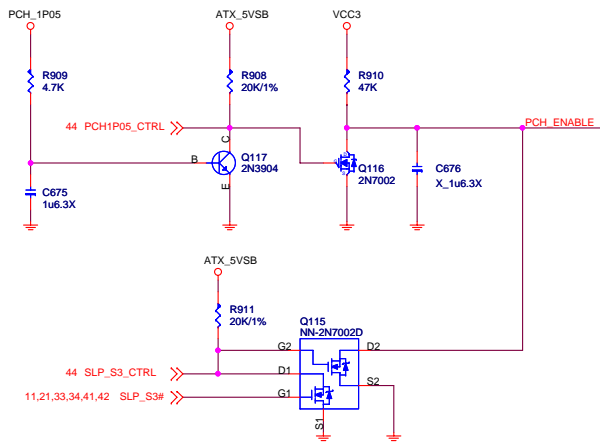
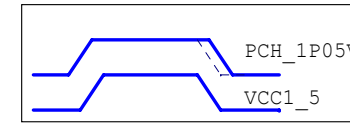
VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH



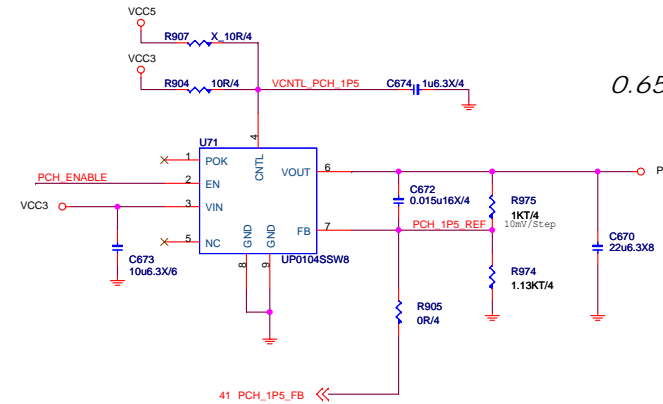
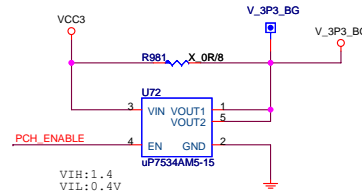
VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH



VCC1\_5\_CTRL\_INPUT:  
0:1P05V low or S3 low  
1:1P05V HIGH and S3 HIGH



0.25A I<sub>max</sub>    I<sub>max</sub>: 0.133A



0.65A I<sub>max</sub>



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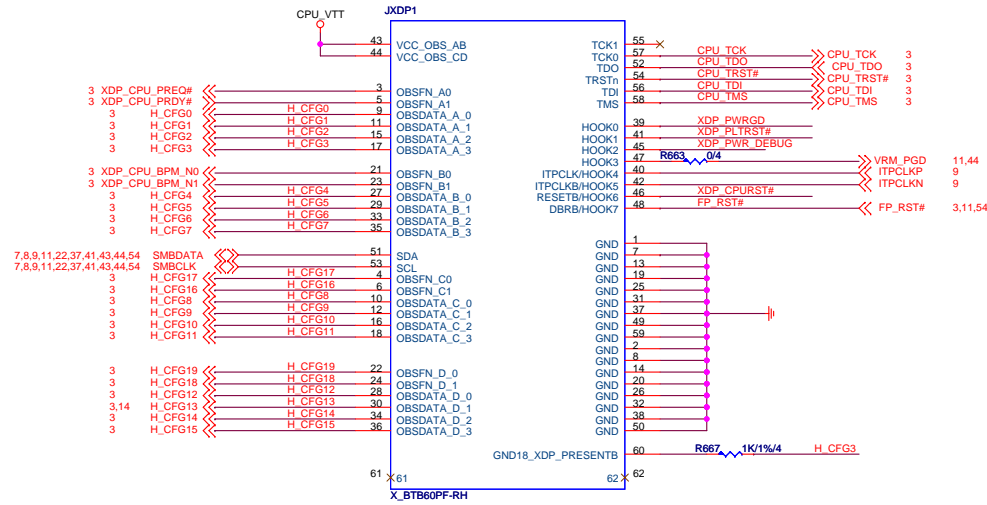
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|-------------------------------|----------------------|-----|
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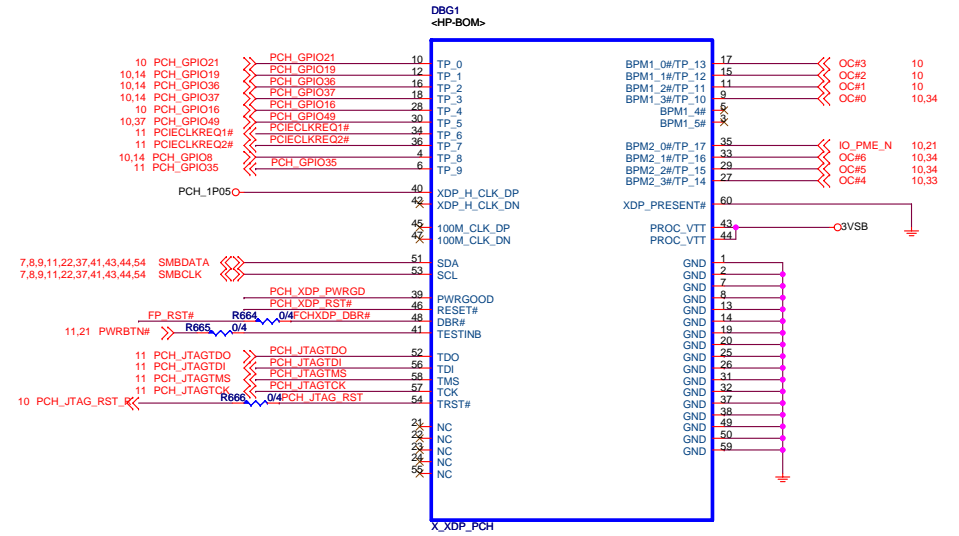




## Reserve debug port 5020

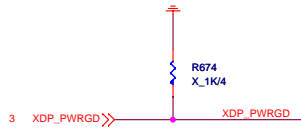


## PCH XDP



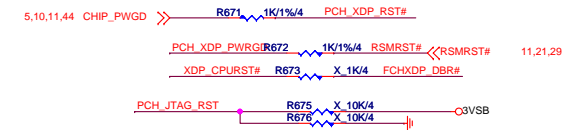
CPU\_TDO R668 51/4 PCH\_1P05  
PLACE NEAR XDP CONNECTOR

21,54 PWRBTIN PWRBTIN R669 0/4 XDP\_PLTRST#  
3 PWR\_DEBUG PWR\_DEBUG R670 0/4 XDP\_PWR\_DEBUG



3,11 CPURST# CPURST# R677 1K1%/4 XDP\_CPURST#

## PCH XDP PWRGD/RESET

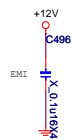


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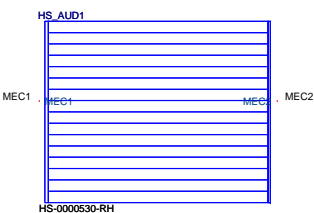
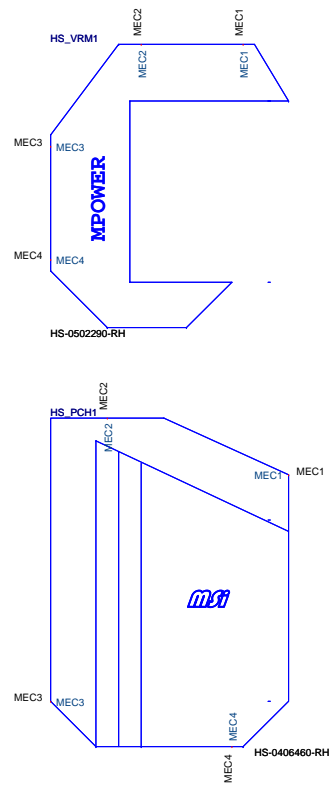




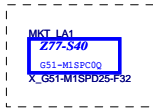
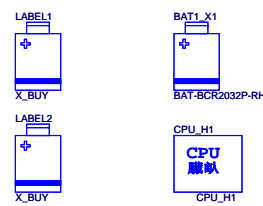
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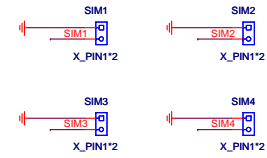
|                               |                                        |                |
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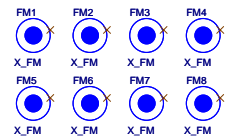
### PCH XDP PWRGD/RESET



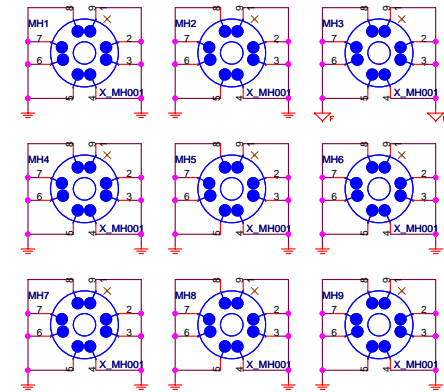
### Simulation



### Optical Fiducial Marks-120



### Mounting Holes



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